乐鑫信息科技

Espressif Systems

ESP8266EX Application Design Guide

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- ✓ ESP8266EX Features
- ✓ ESP8266EX Schematic
- ✓ ESP8266EX Layout
- ✓ Test Board
- ✓ Appendix

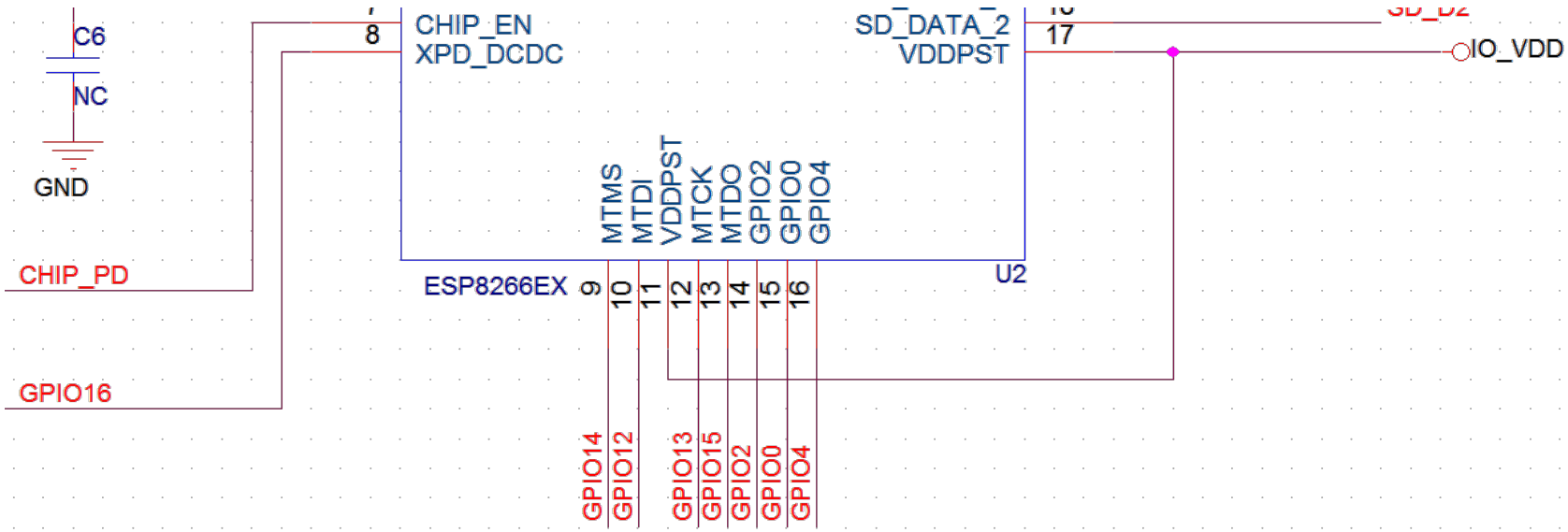
Outline

✓ ESP8266EX Features：

- ✓ External components on ESP8266EX can be reduced to:
  - 7 resistors and capacitors
  - 1 crystal
  - 1 flash
- ✓ All RF parts are integrated and internally self-calibrated when the chip powers on.
- ✓ No special test equipment is needed during production.

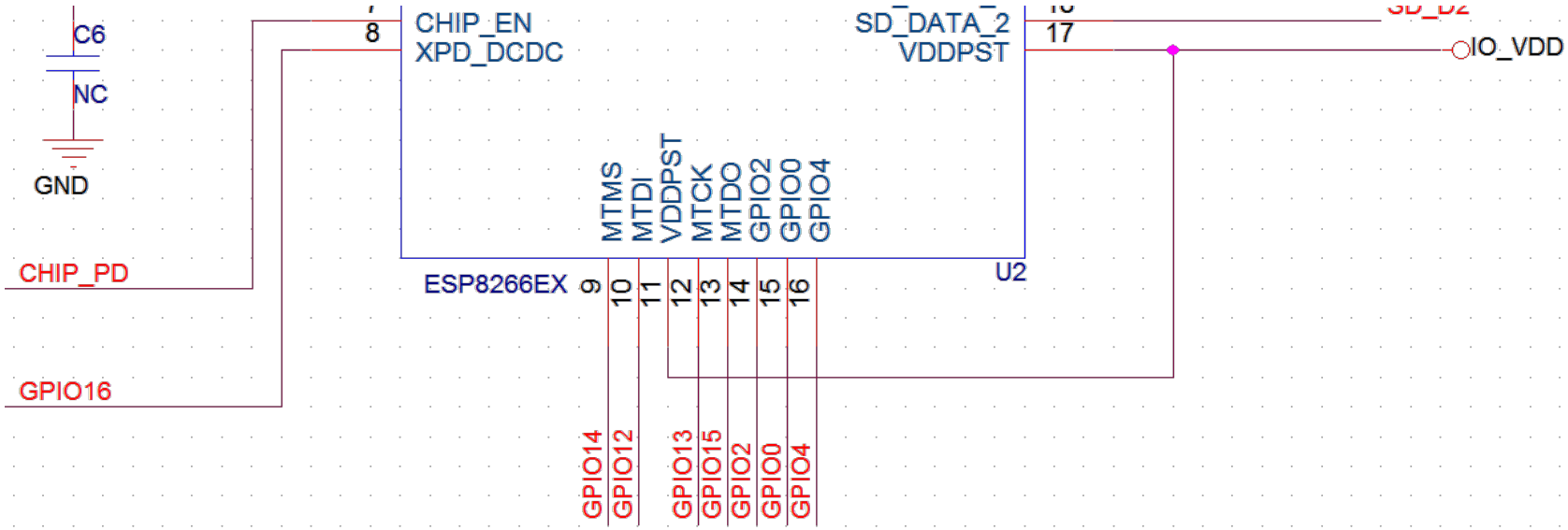
- ✓ Circuit Power On
  - ✓ First power on VDDPST (pin 11, pin 17),

    then power on CHIP_EN (pin 7)
  - ✓ OR power on VDDPST and CHIP_EN at the same time.



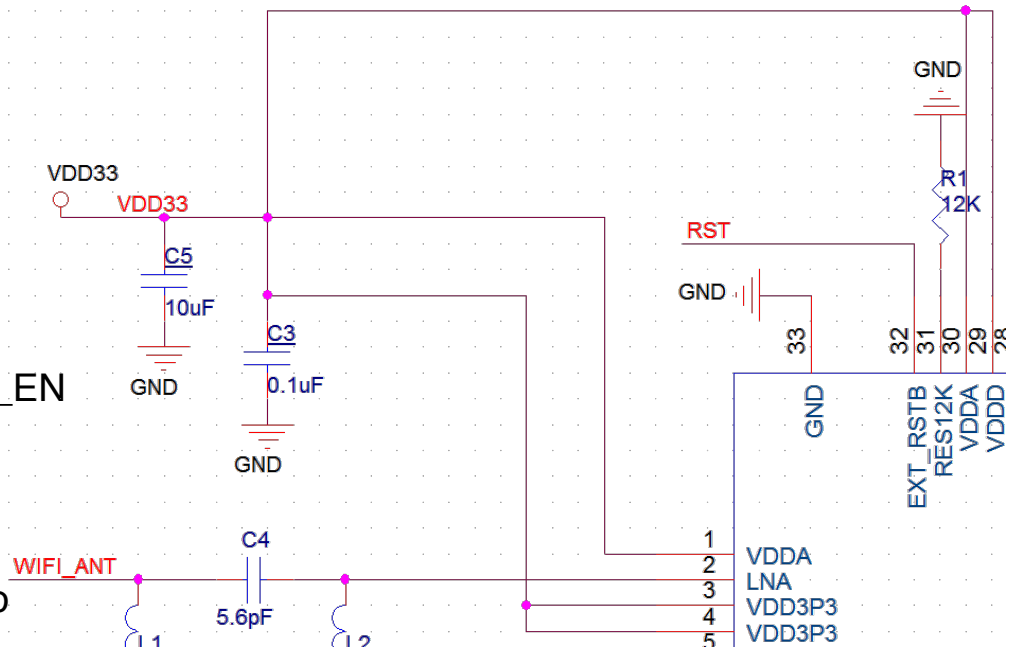
Reference schematic

- ✓ Digital and IO Power Supply
  - ✓ Pin 11, Pin 17 - VDDPST
  - ✓ Voltage: 1.8V ~ 3.3V



Reference schematic

- ✓ Analog Power
  - ✓ Pin 1, Pin 3, Pin 4, Pin 29, Pin 30
  - ✓ Voltage: 3.0V～3.6V



Attention:

1. Recommend using GPIO to control the chip's CHIP_EN pin, so that the power can be kept always on. This will help reduce the need of a switch.
2. If we connect CHIP_EN pin to VCC3V3, we need to add a RC (R=5kΩ, C=1nF) circuit.

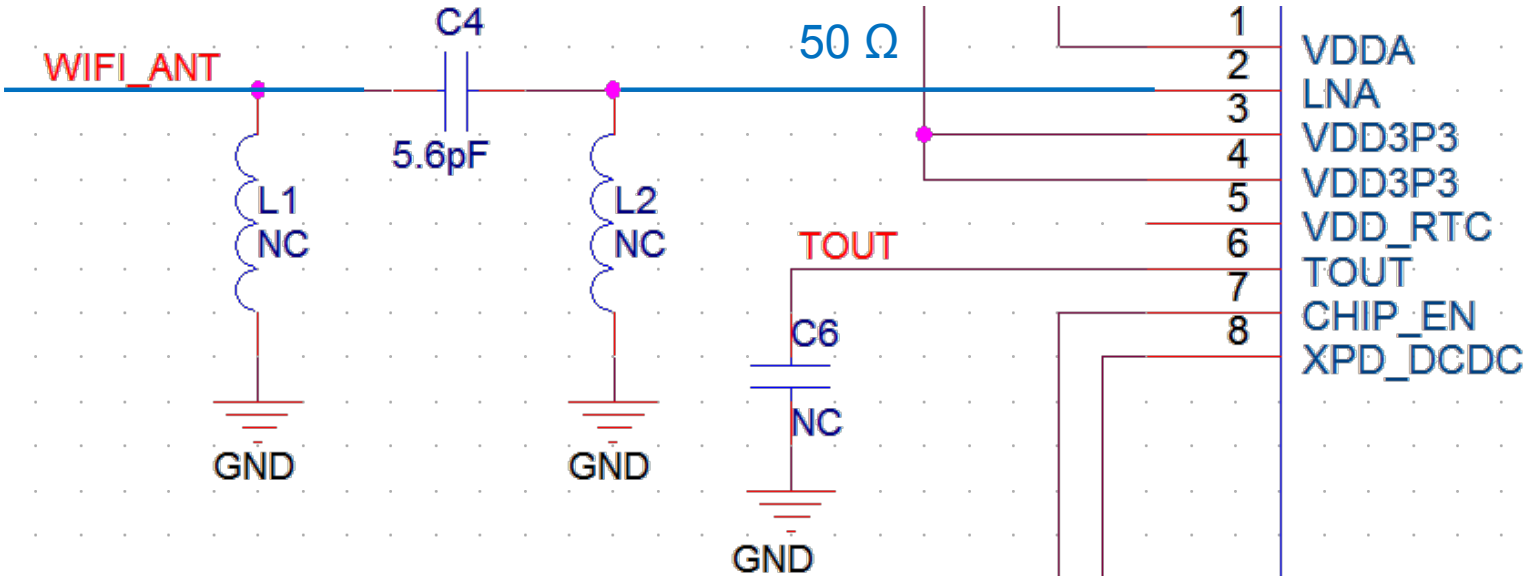
Note that CHIP_EN cannot be left floating.

3. Digital power VDDPST and Analog Power VDDA can be connected together. Add a 10uF decoupling capacitor to ground near chip's power supply pin.
4. Please do not add Ferrite beads in the power trace connected to ESP8266EX.

Reference schematic

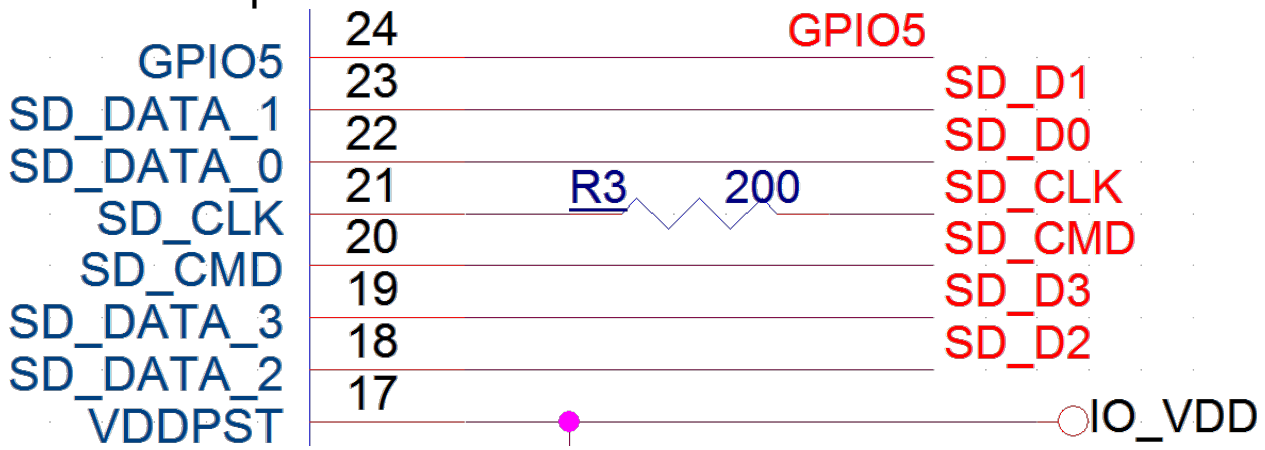
✓ RF Antenna Port

- ✓ The RF port's impedance is 50 Ω. The antenna should be matched to 50 Ω for the best performance.



Reference schematic

- SDIO
  - Add 200 Ω resistors to reduce the noise. If ESP8266EX is far from the CPU, we need to use smaller resistance instead. If space permits, please add matching resistor on all SDIO traces. No need for pull-up resistor in SDIO.
  - In layout design, the resistors should be placed as close as possible to ESP8266EX chip.



Reference schematic

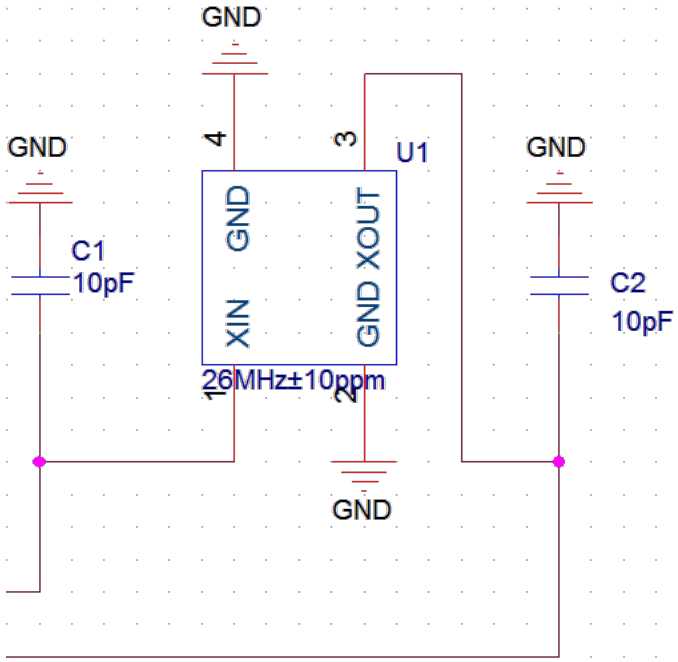
- ✓ CRYSTAL
  - ✓ The maximum allowable frequency offset of crystal is ±10PPM.
  - ✓ The values of C1 and C2 capacitors in crystal input and output is usually in the range of 8.2pF to 12pF. The specific value should be adjusted based on the specifications and refined through testing, to account for parasitics.

Attention:

1、Frequency accuracy of the crystal is critical.

If the frequency deviation is larger than the specified limits, it results in poor iPerf test performance, and degraded sensitivity (like missing some APs during channal scan).

2、Do not use the probe to measure the crystal pin, as it causes frequency deviation.



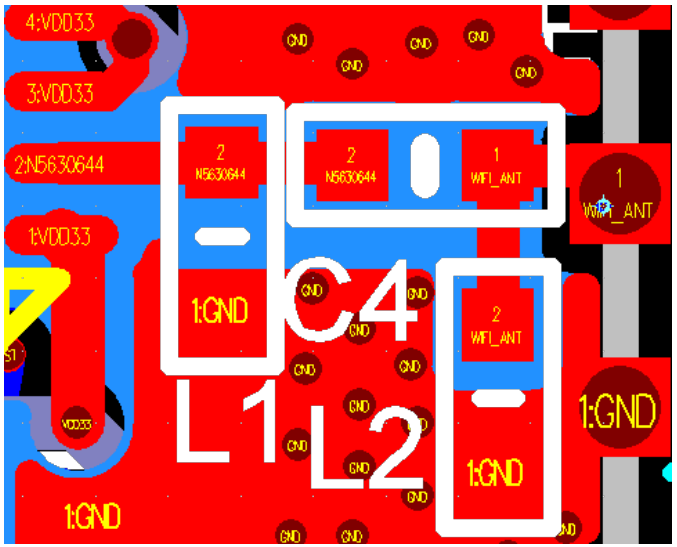
Reference schematic

✓ GENERAL GUIDE LINES

- ✓ 4 Layers are recommend for PCB.
- ✓ If Layer 1 is Signal, then Layer 2 should be GND.
- ✓ Decoupling capacitor C5 should be placed as close to the chip power supply Pin as possible.
- ✓ Width of the trace between Power supply and pin3, 4 should be at least 15mil.
- ✓ No high speed signal traces or power traces below or near the crystal. Traces for 26MHz crystal must be shield well and crystal should be placed as close to the XTAL pins as possible (short lines).

Reference layout design

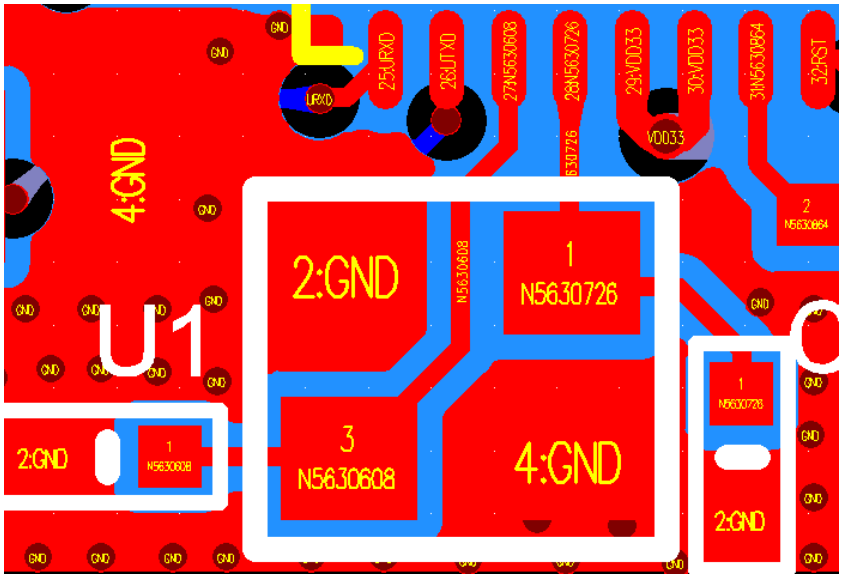
- ✓ RF
  - ✓ RF trace should be 50Ω. Ensure that the signal plane is complete and that it is shielded by vias. The length of RF trace should be as short as possible.
  - ✓ There should be no through vias on RF trace between our chip and antenna. Through vias could be difficult to match and susceptible to noise.



Reference layout design

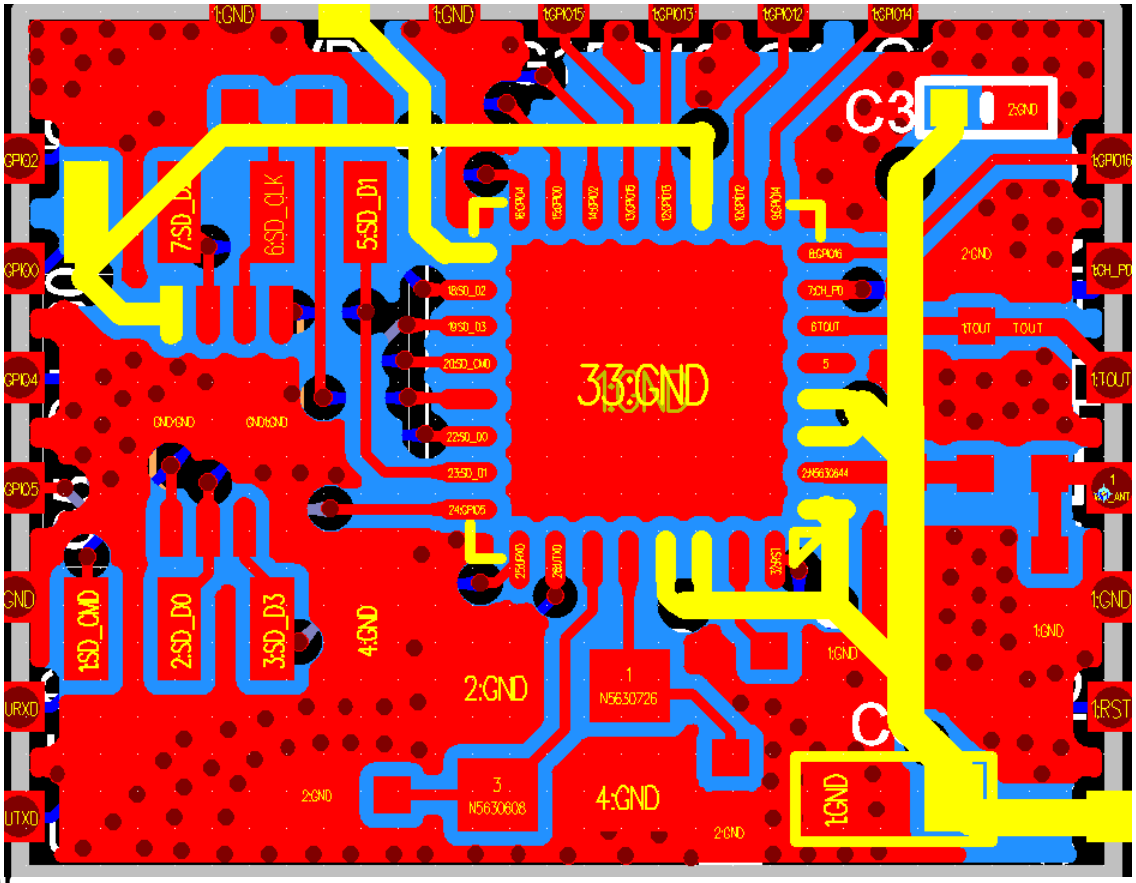
Reference layout design

- ✓ Crystal
  - ✓ Place the crystal close to ESP8266EX to minimize the trace.
  - ✓ Place crystal far way from other signal lines, especially the SDIO signals. Add dense shielding ground vias to separate them.



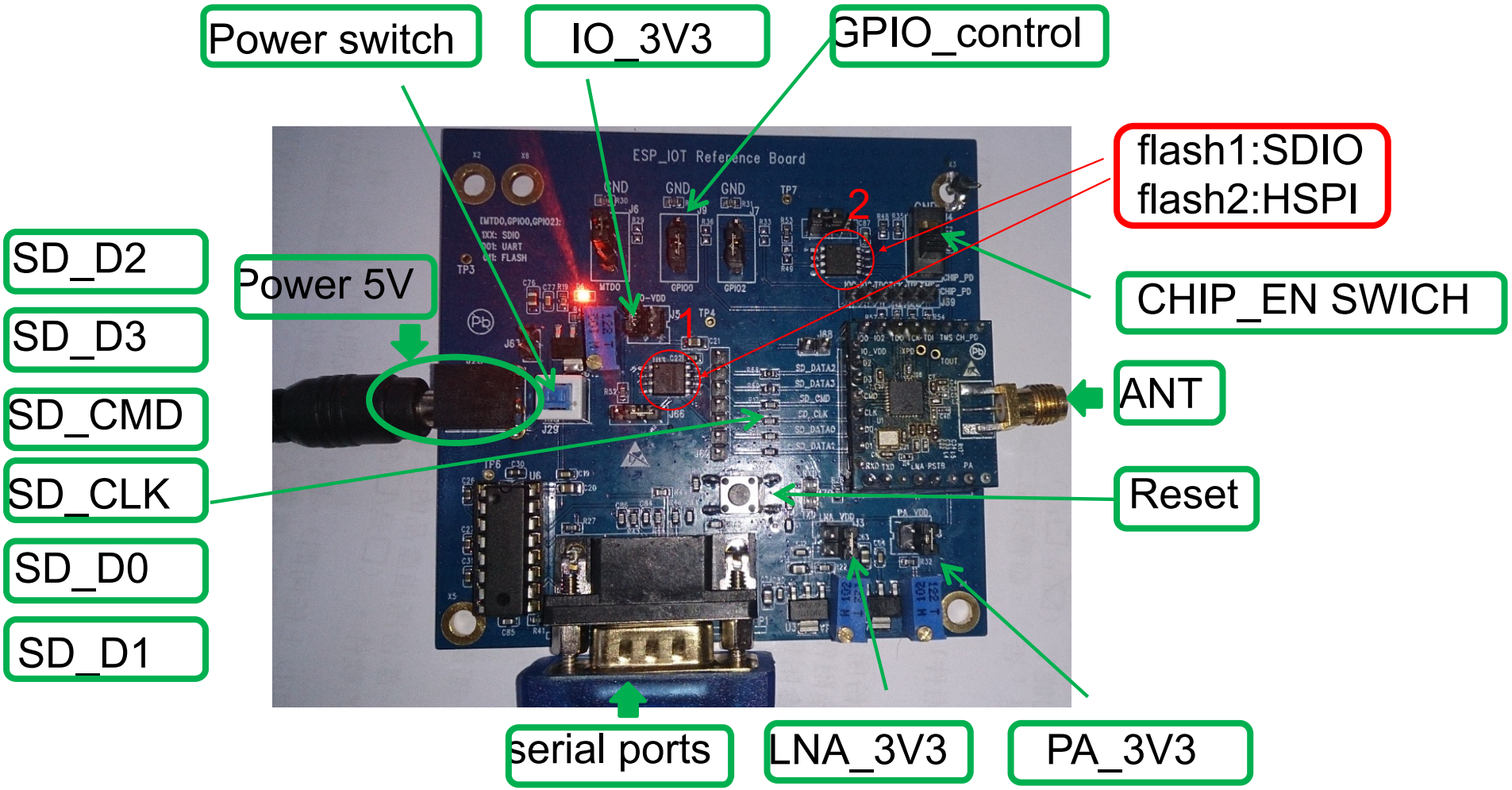
Reference layout design

- ✓ Power trace
  - ✓ The trace should be as wide as possible, and it requires more vias when it has to connect between layers. Place the bypass capacitor close beside the chip.
- ✓ Power Amplifier
  - ✓ The peak current of (pin 3,4) can be as much as 300mA. As such, we cannot ignore the parasitic resistance of the power trace.



- Others:
  - The ground plane of PCB should be as complete as possible. It's not advisable to route power or signal lines directly between the chip or external components.
  - Place vias around the Wi-Fi module circuit to shield it from the other circuit's noise.
  - It is advisable to keep the Wi-Fi chip and antenna away from DRAM, touch panel chips, and LED drivers to minimize digital noise, and optimize the WiFi sensitivity.

Reference layout design



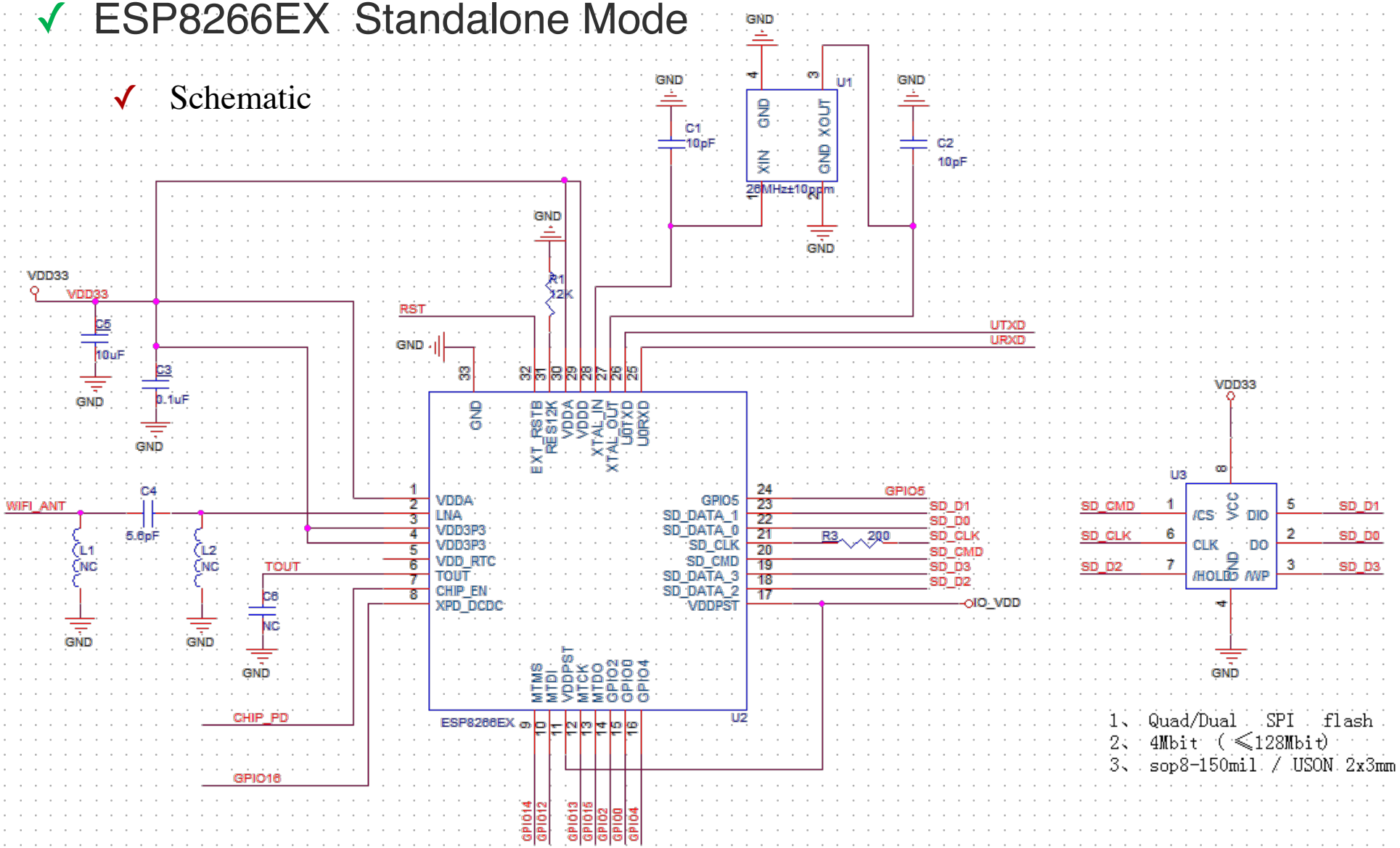
The Interface of Demo Board

Demo board

MTDO	GPIO0	GPIO2	
1	X	X	SDIO / SPI
0	0	1	Uart Download
0	1	1	Flash Boot

GPIO_control

- ESP8266EX Standalone Mode
  - Schematic



Reference schematic

✓ ESP8266EX Standalone Mode

Pin	Name	Desired level during power on	Before first software download	Necessary Function	ANT Switch	Extendable function	Extendable GPIO/I2C
8	XPD_DCDC		Output high	Deep-Sleep	Yes [0]		GPIO16 (optional interal pull-down)
9	MTMS		Input, Internal pull-up resistor			HSPICLK	GPIO14 (optional interal pull-up)
10	MTDI		Input, Internal pull-up resistor			HSPIQ	GPIO12 (optional interal pull-up)
12	MTCK		Input, Internal pull-up resistor			HSPID	GPIO13 (optional interal pull-up)
13	MTDO	Low	Input, Internal pull-up resistor			HSPICS	GPIO15 (optional interal pull-up)
14	GPIO2	High	Output, Many toggles	U1TXD			GPIO2 (optional interal pull-up)
15	GPIO0	High (uart d/l : Low)	Output, Many toggles		Yes [0]	SPICS2	GPIO0 (optional interal pull-up)
16	GPIO4		Input, Internal pull-up resistor				GPIO4 (optional interal pull-up)
18	SD_DATA_2		Input, Hi-Z	SPIHD	Yes	HSPIHD	GPIO9 (optional interal pull-up)
19	SD_DATA_3		Input, Hi-Z	SPIWP	Yes[0]	HSPIWP	GPIO10 (optional interal pull-up)
20	SD_CMD		Input, Hi-Z	SPICS0			No
21	SD_CLK		Input, Hi-Z	SPICLK			No
22	SD_DATA_0		Input, Hi-Z	SPIQ			No
23	SD_DATA_1		Input, Hi-Z	SPID	Yes		No
24	GPIO5		Input, Internal pull-up resistor				GPIO5 (optional interal pull-up)
25	U0RXD		Input, Internal pull-up resistor	U0RXD	Yes		GPIO3 (optional interal pull-up)
26	U0TXD	High	Output, Many toggles	U0TXD	Yes	SPICS1	GPIO1 (optional interal pull-up)

✓ ESP8266EX Standalone Mode

✓ Design Note:

Important 1:

Green: Available GPIO port, but have to consider the notes in red.

Gray: Rarely used in extending GPIO port. SD_DATA_2 and SD_DATA_3 can be used as GPIO ports only when using **dual spi flash**. Only XPD_DCDC support Deep sleep.U0TXD and U0RXD can be used to burn flash.

Blank: Never used in extending GPIO port.

Important 2:

Work mode: GPIO0, GPIO2 and U0TXD should be kept high when powering on the chip. If it is not used, it could be left floating (it has internal pull-up). MTDO should be kept low when powering on the chip.

Uart download mode: GPIO2 and U0TXD should be kept high when powering on the chip. If it is not used, it could be left floating (it has internal pull-up). **MTDO and GPIO0 should be kept low** when powering on the chip.

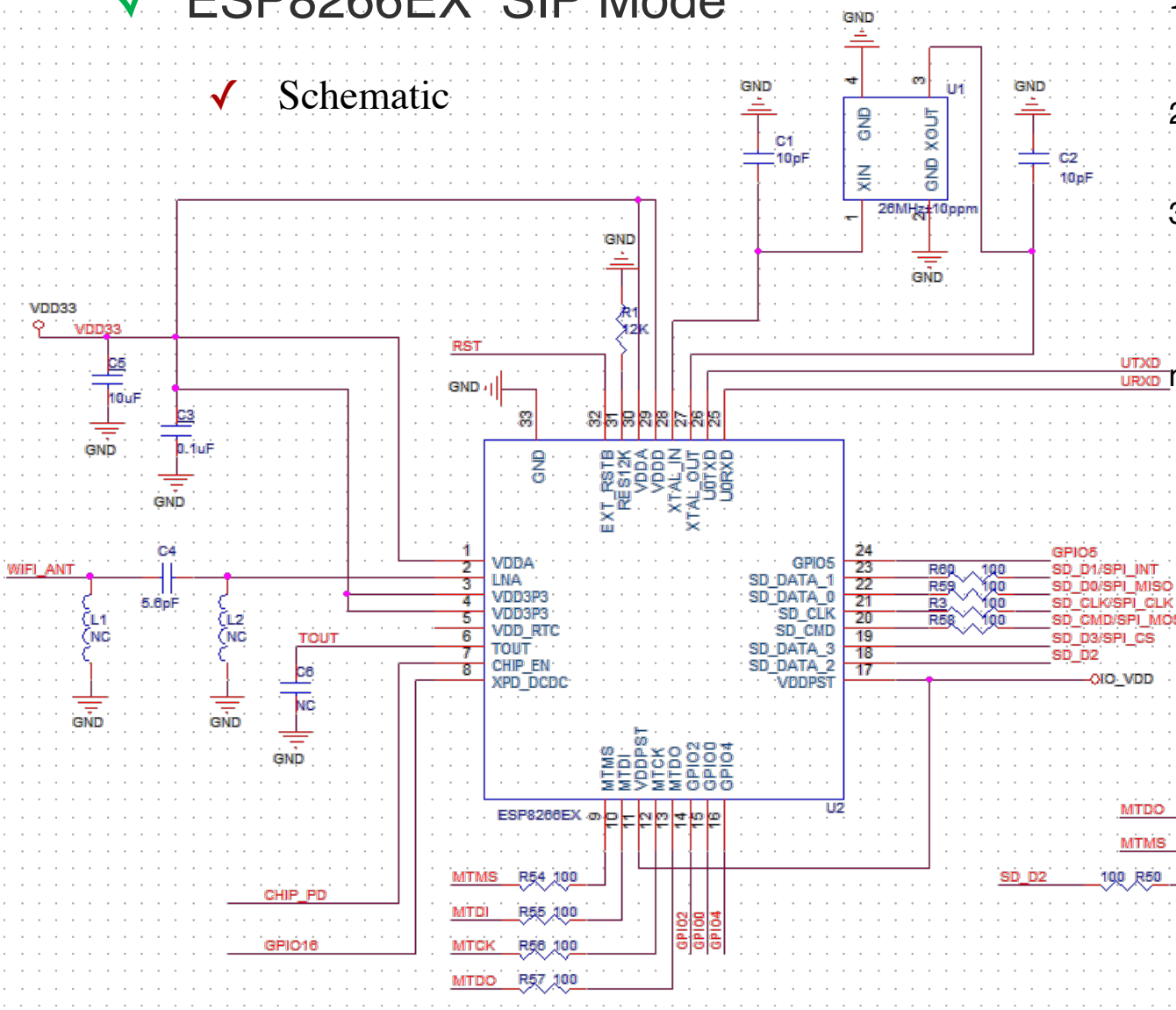
Important 3:

Before downloading the software at first time: GPIO0 output is flipped (output clk signal with the same frequency as Crystal clk). GPIO2 and U0TXD are both output and have many toggles(low speed UART signal). XPD_DCDC output high and the pins of other green and gray highlights are in input state (which has internal pull-up resistor enabled, except for SD_DATA_2 and SD_DATA_3,).

After downloading the software the first time: pins of all green and gray highlights can be set as GPIO, input, input pull-up/pull-down, output high or output low.

✓ ESP8266EX SIP Mode

✓ Schematic



1、 Quad/Dual SPI flash
2、 4Mbit (≤128Mbit)
3、 sop8-150mil / USON 2x3mm

Note：

1. CHIP_PD, as an enable pin, should be connected to a GPIO of Host CPU.

2. Dual SPI Flash(DIO/DOUT):
   Remove R50,R47,R51 and keep R49, R48.

3.Quad SPI Flash(QIO/QOUT):
   Remove R48,R49 and keep R47,R50,R51.
   a.1 bit SDIO: No need to connect SD_D2 and SD_D3 to Host.
   b.SPI: SD_D3 is used as SPI_CS and no need to be connected to Host.

Reference schematic

✓ ESP8266EX SPI-Slave Mode

Pin	Name	Desired level during power on	Before first software download	Necessary Function	ANT Switch	extendable GPIO
8	XPD_DCDC		Output high		Yes [0]	GPIO16 (optional interal pull-
9	MTMS		Input, Internal pull-up	HSPICLK		GPIO14 (optional interal pull-up)
10	MTDI		Input, Internal pull-up resistor	HSPIQ		GPIO12 (optional interal pull-up)
12	MTCK		Input, Internal pull-up resistor	HSPID		GPIO13 (optional interal pull-up)
13	MTDO	High (uart d/l：Low)	Input, Internal pull-up resistor	HSPICS		GPIO15 (optional interal pull-up)
14	GPIO2		Output, Many toggles	Add testpoint：U1TXD		GPIO2 (optional interal pull-up)
15	GPIO0	(uart d/l：Low)	Output, Many toggles		Yes [0]	GPIO0 (optional interal pull-up)
16	GPIO4		Input, Internal pull-up			GPIO4(optional interal pull-up)
18	SD_DATA_2		Input, Hi-Z	HSPIHD	Yes	GPIO9 (optional interal pull-up)
19	SD_DATA_3		Input, Hi-Z	SPI_SLAVE_CS（or pull down)	Yes [0]	GPIO10 (optional interal pull-up)
20	SD_CMD		Input, Hi-Z	SPI_SLAVE _MOSI		No
21	SD_CLK		Input, Hi-Z	SPI_SLAVE _CLK		No
22	SD_DATA_0		Input, Hi-Z	SPI_SLAVE _MISO		No
23	SD_DATA_1		Input, Internal pull-up		Yes	No
24	GPIO5		Input, Internal pull-up			GPIO5(optional interal pull-up)
25	U0RXD		Input, Internal pull-up	U0RXD	Yes	GPIO3 (optional interal pull-up)
26	U0TXD	HIgh	Output, Many toggles	U0TXD	Yes	GPIO1 (ptional interal pull-up)

✓ ESP8266EX SPI-Slave Mode

✓ Design Note:

Important 1:
Green: Available, but have to consider the red mark.
Gray: Rarely used in extending GPIO port. SD_DATA_2 and SD_DATA_3 can be used as GPIO ports only when using **dual spi flash**. SD_DATA_3 should be kept low during downloading firmware.
Blank: Never used in extending GPIO port.
Important 2:
Work mode: MTDO and U0TXD should be kept high when powering on the chip. If it is not used, it could be left floating (it has internal pull-up). MTDO should be kept low when powering on the chip.
Flash burning can use SPI Slave interface, downloading from the host, this is the same as the normal mode.
Uart download mode: GPIO2 and U0TXD should be kept high when powering on the chip. If it is not used, it could be left floating (it has internal pull-up). **MTDO and GPIO0 should be kept low** when powering on the chip.
Important 3:
Before downloading the software at first time: GPIO0 is output and flipped(output clk signal with the same frequency as Crystal clk). GPIO2 and U0TXD are both output and have many toggles(low speed uart signal).XPD_DCDC output high and the pins of other green and gray highlights are in inputting state (except SD_DATA_2 and SD_DATA_3, which has internal enable pull-up resistor).
After downloading the software at the first time: pins of all green and gray highlights can be set as GPIO, input, input pull-up/pull-down, output high or output low.

Thanks!