Espressif IOT ESP8266EX

A Beginner's Guide

Version 0.7

Espressif Systems IOT Team

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1. General Overview of ESP8266EX

1.1. Introduction

Espressif Systems' Smart Connectivity Platform (ESCP) is a set of high performance, high integration wireless SOCs, designed for space and power constrained mobile platform designers. It provides unsurpassed ability to embed Wi-Fi capabilities within other systems, or to function as a standalone application, with the lowest cost, and minimal space requirement.

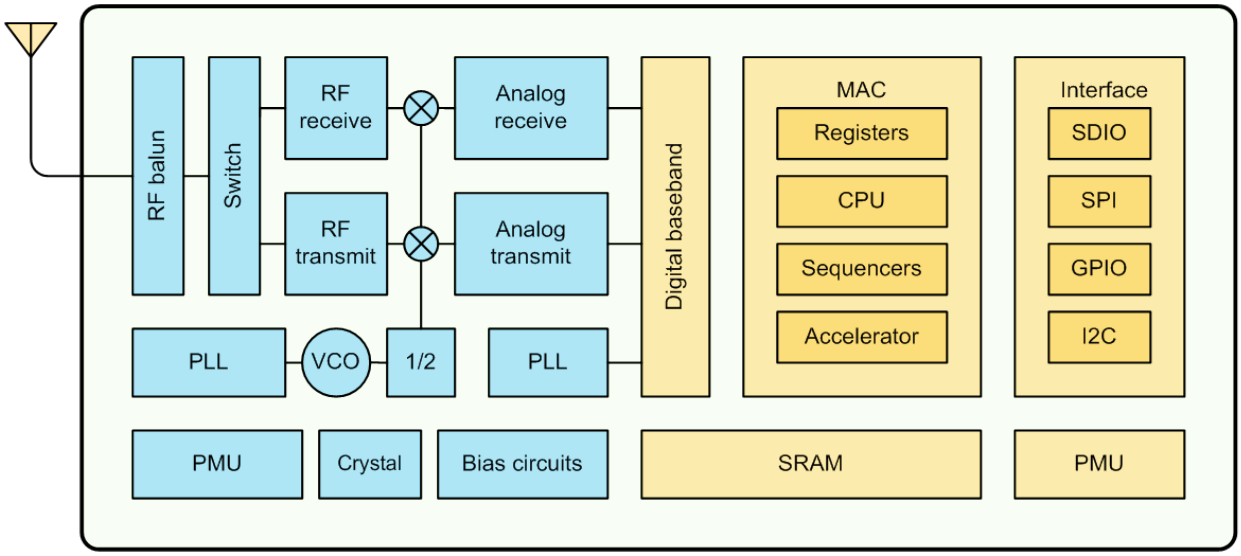


Figure 1: ESP8266EX Block Diagram

ESP8266EX offers a complete and self-contained Wi-Fi networking solution; it can be used to host the application or to offload Wi-Fi networking functions from another application processor.

When ESP8266EX hosts the application, it boots up directly from an external flash. In has integrated cache to improve the performance of the system in such applications.

Alternately, serving as a Wi-Fi adapter, wireless internet access can be added to any micro controller-based design with simple connectivity (SPI/SDIO or I2C/UART interface).

ESP8266EX is among the most integrated WiFi chip in the industry; it integrates the antenna switches, RF balun, power amplifier, low noise receive amplifier, filters, power management modules, it requires minimal external circuitry, and the entire solution, including front-end module, is designed to occupy minimal PCB area.

ESP8266EX also integrates an enhanced version of Tensilica's L106 Diamond series 32-bit processor, with on-chip SRAM, besides the Wi-Fi functionalities. ESP8266EX is often integrated with external sensors and other application specific devices through its GPIOs; sample codes for such applications are provided in the software development kit (SDK).

Espressif Systems' Smart Connectivity Platform (ESCP) demonstrates sophisticated system-level features include fast sleep/wake context switching for energy-efficient VoIP, adaptive radio biasing for low-power operation, advance signal processing, and spur cancellation and radio co-existence features for common cellular, Bluetooth, DDR, LVDS, LCD interference mitigation.

1.2. Features

- 802.11 b/g/n
- Wi-Fi 2.4 GHz, support WPA/WPA2
- Super small module size (11.5mm x 11.5mm)
- Integrated 10-bit ADC
- Integrated TCP/IP protocol stack
- Integrated TR switch, balun, LNA, power amplifier and matching network
- Integrated PLL, regulators, and power management units
- +20dBm output power in 802.11b mode
- Supports antenna diversity
- Deep sleep power <10uA, Power down leakage current < 5uA
- Integrated low power 32-bit MCU
- SDIO 2.0, SPI, UART
- STBC, 1x1 MIMO, 2x1 MIMO
- A-MPDU & A-MSDU aggregation & 0.4ìs guard interval
- Wake up and transmit packets in < 2ms
- Standby power consumption of < 1.0mW (DTIM3)
- Operating temperature range -40C ~ 125C

1.3. Parameters

Categories	Items	Values
WiFi Paramters	Certificates	CCC/FCC/CE/TELEC/SRRC
	WiFi Protocles	802.11 b/g/n
	Frequency Range	2.4G-2.5G (2400M-2483.5M)
	Tx Power	802.11 b: 20 dBm
		802.11 g: 17 dBm
		802.11 n: 14 dBm
	Rx Sensitivity	802.11 b: (11Mbps) -91dbm
		802.11 g: (54Mbps) -75dbm
		802.11 n: (MCS7) -72dbm
	Types of Antenna	PCB Trace, External, IPEX Connector, Ceramic Chip
Hardware Paramaters	Peripheral Bus	UART/SDIO/SPI/I2C/I2S/IrDA
		GPIO/PWM
	Operating Voltage	3.0~3.6V
	Operating Current	Average value: 80mA
	Operating Temperature Range	-40°~125°
	Ambient Temperature Range	Normal temperature
	Package Size	5x5mm
	External Interface	N/A
Software Parameters	Wi-Fi mode	station/softAP/SoftAP+station
	Security	WPA/WPA2
	Encryption	WEP/TKIP/AES
	Firmware Upgrade	UART Download / OTA (via network)
	Ssoftware Development	Supports Cloud Server Development / SDK for custom firmware development

	Network Protocols	IPv4, TCP/UDP/HTTP/FTP
	User Configuration	AT Instruction Set, Cloud Server, Android/ iOS App

Table 1 Parameters of ESP8266EX

1.4. Major Applications

Major fields of ESP8266EX applications to Internet-of-Things include:

- Home Appliances
- Home Automation
- Smart Plug and lights
- Mesh Network
- Industrial Wireless Control
- Baby Monitors
- IP Cameras
- Sensor Networks
- Wearable Electronics
- Wi-Fi Location-aware Devices
- Security ID Tags
- Wi-Fi Position System Beacons

2. Hardware Overview

2.1. Terminal Configuration and Functions

The pin assignments for 32-pin QFN package is illustrated in Fig.2.

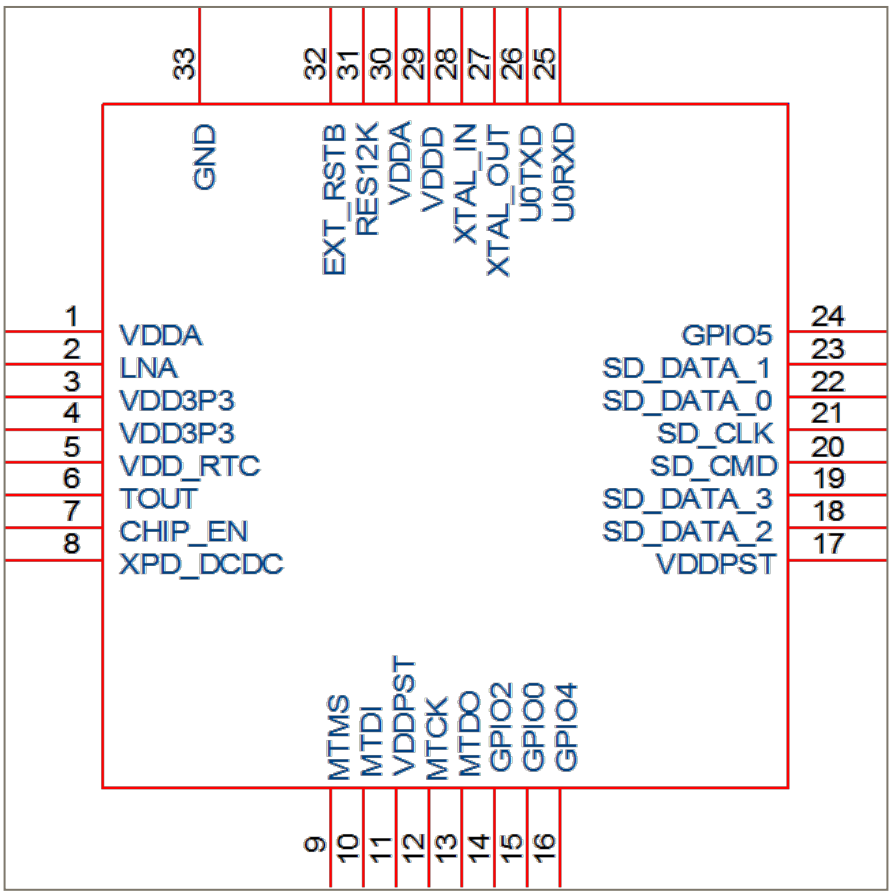


Figure 2 Pin Assignments

Table.2 below presents an overview on the general pin attributes and the functions of each pin.

Pin	Name	Type	Function
1	VDDA	P	Analog Power 3.0 ~3.6V
2	LNA	I/O	RF Antenna Interface, Chip Output Impedance=50Ω No matching required but we recommend that the π-type matching network is retained.
3	VDD3P3	P	Amplifier Power 3.0~3.6V
4	VDD3P3	P	Amplifier Power 3.0~3.6V
5	VDD_RTC	P	NC(1.1V)
6	TOUT	I	ADC Pin
7	CHIP_EN	I	Chip Enable. High: On, chip works properly; Low: Off, small current
8	XPD_DCDC	I/O	Deep-Sleep Wakeup； GPIO16
9	MTMS	I/O	GPIO14; HSPICLK
10	MTDI	I/O	GPIO12;HSPIQ
11	VDDPST	P	Digital/IO Power Supply (1.8V~3.3V)
12	MTCK	I/O	GPIO13;HSPID
13	MTDO	I/O	GPIO15;HSPICS
14	GPIO2	I/O	UART Tx during flash programming; GPIO2
15	GPIO0	I/O	GPIO0;SPICS2
16	GPIO4	I/O	GPIO4
17	VDDPST	P	Digital/IO Power Supply (1.8V~3.3V)
18	SDIO_DATA_2	I/O	Connect to SD_D2 (Series R: 200Ω);SPIHD; HSPIHD
19	SDIO_DATA_3	I/O	Connect to SD_D3 (Series R: 200Ω); SPIWP; HSPIWP
20	SDIO_CMD	I/O	Connect to SD_CMD (Series R: 200Ω); SPICS0
21	SDIO_CLK	I/O	Connect to SD_CLK (Series R: 200Ω); SPICLK
22	SDIO_DATA_0	I/O	Connect to SD_D0 (Series R: 200Ω); SPIQ
23	SDIO_DATA_1	I/O	Connect to SD_D1 (Series R: 200Ω); SPID
24	GPIO5	I/O	GPIO5
25	U0RXD	I/O	UART Rx during flash programming; GPIO3
26	U0TXD	I/O	UART Tx during flash progamming; GPIO1; SPICS1

27	XTAL_OUT	I/O	Connect to crystal oscillator output, can be used to provide BT clock input
28	XTAL_IN	I/O	Connect to crystal oscillator input
29	VDDD	P	Analog Power 3.0~3.6V
30	VDDA	P	Analog Power 3.0~3.6V
31	RES12K	I	Connect to series R 12kΩ to ground
32	EXT_RSTB	I	External reset signal (Low: Active)

Table 2 Attributes and Functions of Pins

Note: GPIO2, GPIO0, MTDO can be configurable as 3-bit SDIO mode.

2.2. Electrical Characteristics

Parameters		Conditions	Min	Typical	Max	Unit
Storage Temperature Range			-40	Normal	125	°C
Maximum Soldering Temperature		IPC/JEDEC J-STD-020			260	°C
Working Voltage Value			3.0	3.3	3.6	V
I/O	V_{IL}/V_{IH}		-0.3/0.75V_{IO}		0.25V_{IO}/3.6	V
	V_{OL}/V_{OH}		N/0.8V_{IO}		0.1V_{IO}/N	
	I_{MAX}				12	mA
Electrostatic Discharge (HBM)		TAMB=25°C			2	KV
Electrostatic Discharge (CDM)		TAMB=25°C			0.5	KV

Table 3 ESP8266EX Electrical Characteristics

Parameters	Min	Typical	Max	Unit
Tx802.11b, CCK 11Mbps, P OUT=+17dBm		170		mA
Tx 802.11g, OFDM 54Mbps, P OUT =+15dBm		140		mA
Tx 802.11n, MCS7, P OUT =+13dBm		120		mA
Rx 802.11b, 1024 bytes packet length , -80dBm		50		mA
Rx 802.11g, 1024 bytes packet length, -70dBm		56		mA
Rx 802.11n, 1024 bytes packet length, -65dBm		56		mA
Modem-Sleep①		15		mA
Light-Sleep②		0.9		mA
Deep-Sleep③		10		uA
Power Off		0.5		uA

Table 4 Description on Power Consumption

①: Modem-Sleep requires the CPU to be working, as in PWM or I2S applications. According to 802.11 standards (like U-APSD), it saves power to shut down the Wi-Fi Modem circuit while maintaining a Wi-Fi connection with no data transmission. E.g. in DTIM3, to maintain a sleep 300ms-wake 3ms cycle to receive AP's Beacon packages, the current is about 15mA

②: During Light-Sleep, the CPU may be suspended in applications like Wi-Fi switch. Without data transmission, the Wi-Fi Modem circuit can be turned off and CPU suspended to save power according to the 802.11 standard (U-APSD). E.g. in DTIM3, to maintain a sleep 300ms-wake 3ms cycle to receive AP's Beacon packages, the current is about 0.9mA.

③: Deep-Sleep does not require Wi-Fi connection to be maintained. For application with long time lags between data transmission, e.g. a temperature sensor that checks the temperature every 100s, sleep 300s and waking up to connect to the AP (taking about 0.3~1s), the overall average current is less than 1mA.

2.3. Memory Organisation

1. MCU

ESP8266EX is embedded with Tensilica L106 32-bit micro controller (MCU), which features extra low power consumption and 16-bit RSIC. The CPU clock speed is 80MHz. It can also reach a maximum value of 160MHz. Real Time Operation System (RTOS) is enabled. According to the current version of SDK, only 20% of MIPS has been occupied by the WiFi stack, the rest can all be used for application development. The following interfaces can be used to connect to the MCU embedded in ESP8266EX:

- Programmable RAM/ROM interfaces (iBus), which can be connected with memory controller, and can also be used to visit external flash;

- Data RAM interface (dBus), which can connected with memory controller;
- AHB interface, can be used to visit the register.

2. Internal SRAM and ROM

ESP8266EX WiFi SoC is embedded with memory controller, including SRAM and ROM. MCU can visit the memory units through iBus, dBus, and AHB interfaces. All memory units can be visited upon request, while a memory arbiter will decide the running sequence according to the time when these requests are received by the processor.

According to our current version of SDK provided, SRAM space that is available to users is assigned as below:

- **RAM size < 45kB,** that is to say, when ESP8266EX is working under the station mode and is connected to the router, programmable space accessible to user in heap and data section is around 45kB.)
- There is no programmable ROM in the SoC, therefore, user program must be stored in an external SPI flash.

3. External SPI Flash

An external SPI flash is used together with ESP8266EX to store user program. The size of a SOP8 packaged flash memory applied in our current Demo is 512KB, while definable user program is less than 64KB. If larger definable storage space is required, you'd better choose a SPI flash with larger memory size. Theoretically speaking, up to 16MB is supported.

The minimum flash memory that can be supported:

- OTA is disabled: the minimum flash memory that can be supported is 256kB;
- OTA is enabled: the minimum flash memory that can be supported is 512kB.

ESP8266EX can support a several SPI modes including Standard SPI, Dual SPI, and Quad SPI. Therefore, when you are downloading some programs into the flash, please choose the correct SPI mode, otherwise, the programs that you downloaded may not work in the right way.

2.4. Pin Definitions

1. General Purpose Input/Output Interface (GPIO)

There are up to 16 GPIO pins. They can be assigned to various functions by the firmware. Each GPIO can be configured with internal pull-up/down, input available for sampling by a software register, input triggering an edge or level CPU interrupt, input triggering a level wakeup interrupt, open-drain or push-pull output driver, or output source from a software register, or a sigma-delta PWM DAC.

These pins are multiplexed with other functions such as I2C, I2S, UART, PWM, IRDA, etc.

Data I/O soldering pad is bidirectional and tri-state that include data input and output controlling buffer. Besides, I/O can be set as a specific state and remains like this. For example, if you intend to lower the power consumption of the chip, all data input and output enable signals can be set as remaining low power state. You can transport some specific state into the I/O. When the I/O is not powered by external circuits, the I/O will remain to be the state that it was used the last time. Some positive feedback is generated by the state-remaining function of the pins, therefore, if the external driving power must be stronger than the positive feedback. Even so, the driving power that is needed is within 5uA.

Variables	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	-0.3	$0.25 \times V_{IO}$	V
Input High Voltage	V_{IH}	$0.75 \times V_{IO}$	3.3	V
Input Leakage Current	I_{IL}		50	nA
Output Low Voltage	V_{OL}		$0.1 \times V_{IO}$	V
Output High Voltage	V_{OH}	$0.8 \times V_{IO}$		V
Input Pin Resistance Value	C_{pad}		2	pF
VDDIO	V_{IO}	1.8	3.3	V
Maximum Driving Power	I_{MAX}		12	mA
Temerpature	T_{amb}	-40	125	°C

Table 5 Pin Definitions of GPIOs

2. Secure Digital Input/Output Interface (SDIO)

One Slave SDIO has been defined by ESP8266EX. 4bit 25MHz SDIO v1.1 and 4bit 50MHz SDIO v2.0 are supported.

Pin Name	Function Name	Type	Pin Num
SDIO_CLK	SDIO_CLK	I	21
SDIO_DATA0	SDIO_DATA0	I/O/T	22
SDIO_DATA1	SDIO_DATA1	I/O/T	23
SDIO_DATA_2	SDIO_DATA_2	I/O/T	18
SDIO_DATA_3	SDIO_DATA_3	I/O/T	19
SDIO_CMD	SDIO_CMD	I/O/T	20

Table 6 Pin Definitions of SDIOs

3. Serial Peripheral Interface (SPI/HSPI)

Three SPIs, including one general Slave/Master SPI, one Slave SDID/SPI, and one Slave/Master HSPI have been defined by ESP8266EX, the pin definitions are are described below:

General SPI (Master/Slave)

Pin Name	Function Name	Type	Pin Num
SDIO_CLK	SPICLK	I/O/T	21
SDIO_DATA0	SPIQ/MISO	I/O/T	22
SDIO_DATA1	SPID/MOSI	I/O/T	23
SDIO_DATA_2	SPIHD	I/O/T	18
SDIO_DATA_3	SPIWP	I/O/T	19
SDIO_CMD	SPICS0	I/O/T	20

Table 7 Pin Definitions of General SPIs

SDIO /SPI (Slave)

Pin Name	Function Name	Type	Pin Num
SDIO_CLK	SPI_SLAVE_CLK	I	21
SDIO_DATA0	SPI_SLAVE_MISO	I/O/T	22
SDIO_DATA1	SPI_SLAVE_INT	I/O/T	23
SDIO_DATA_2	NC	I/O/T	18
SDIO_DATA_3	SPI_SLAVE_CS	I/O/T	19
SDIO_CMD	SPI_SLAVE_MOSI	I/O/T	20

Table 8 Pin Definitions of SDIOs/SPIs (Slave)

HSPI (Master/Slave)

Pin Name	Function Name	Type	Pin Num
MTMS	HSPICLK	I/O/T	9
MTDI	HSPIQ/MISO	I/O/T	10
MTCK	HSPID/MOSI	I/O/T	12
MTDO	HPSICS	I/O/T	13

Table 9 Pin Definitions of H SPIs (Master/Slave)

Note:

- The SPI mode is operational, and the CLK speed can reach up to 80MHz.
- HSPI mode is also operational, the CLK speed of which is the same with standard SPI. However, there is no linked list DMA (Direct Memory Access), therefore, the data processing speed will be restrained if this operation mode is chosen.

4. Inter-integrated Circuit Interface (I2C)

One I2C, which is mainly used to connect with micro controller and other peripheral equipment such as sensors, is defined by ESP8266EX. If you want more than one I2C interfaces, please contact us on how to achieve this kind of configuration. The present pin definition of I2C is as defined below:

Pin Name	Function Name	Type	Pin Num
MTMS	I2C_SCL	I/O/T	9
GPIO2	I2C_SDA	I/O/T	14

Table 10 Pin Definitions of I2C

Both I2C-Master and I2C-Slave are supported. I2C interface functionality can be realized via software programming, the CLK speed of under this operation mode can be up to around 100KHz at most.

5. I2S

One I2S interface, which is mainly applied in data collection, processing, and transmission of audio data, is defined by ESP8266EX. The pin definition of I2S is as defined below:

Pin Name	Function Name	Type	Pin Num
MTDI	I2SI_DATA	I/O/T	10
MTCK	I2SI_BCK	I/O/T	12
MTMS	I2SI_WS	I/O/T	9
MTDO	I2SO_BCK	I/O/T	13
U0RXD	I2SO_DATA	I/O/T	25
GPIO2	I2SO_WS	I/O/T	14

Table 11 Pin Definitions of I2S

I2S functionality can be realized via software programming, the GPIOs that will be used are multiplexed.

6. Universal Asynchronous Receiver Transmitter (UART)

Two UART interfaces, UART0 and UART1, have been defined by ESP8266EX, the definitions are as below:

Pin Type	Pin Name	Function Name	Type	Pin Num
UART0	U0RXD	U0RXD	I	25
	U0TXD	U0TXD	O	26
	U0RTS	MTDO	O	13
	U0CTS	MTCK	I	12
UART1	GPIO2	U1TXD	O	14

Table 12 Pin Definitions of UART Interfaces

Data transfers to/from UART interfaces can be implemented via hardware. The data transmission speed via UART interfaces can reach 115200*40 (4.5Mbps).

UART0 can be for communication. It supports fluid control. Since UART1 features only data transmit signal (Tx), it is usually used for printing log.

Notes: By default UART0 will output some printed information when the device is powered on and is booting up. The baud rate of the printed information is closely related to the frequency of the external crystal oscillator. If the frequency of the crystal oscillator is 40MHz, then the baud rate for printing is 115200; if the frequency of the crystal oscillator is 26MHx, then the baud rate for printing is 74880. If the printed information exerts any influence on the functionality of your device, you'd better block the printing during the power-on period by changing (`U0TXD,U0RXD`) to (`MTDO,MTCK`).

7. Pulse-Width Modulation (PWM)

Four PWM output interfaces have been defined by ESP8266EX. They can be extended by oneself. The present pin definitions of the PWM interfaces are as below:

Pin Name	Function Name	Type	Pin Num
MTDI	PWM0	O	10
MTDO	PWM1	O	13
MTMS	PWM2	O	9
GPIO4	PWM3	O	16

Table 13 Pin Definitions of PWM Interfaces

The functionality of PWM interfaces can be implemented via software programming. For example, in the LED smart light demo, the function of PWM is realized by interruption of the timer, the duty ratio is between 0 and 100%, the depth is 8-bit, 1/256, the frequency range is between 100Hz and 1KHz. Hardware sigma-delta can generate 312KHz, 0 to 100% (1/256) wave.

8. Infrared Data Association (IRDA)

Currently, only one IRDA interface is defined, the definition of which is as shown below:

Pin Name	Function Name	Type	Pin Num
MTMS	IRDA Rx	I	9
GPIO5	IRDA Tx	O	24

Table 14 Pin Definitions of IRDA

The functionality of IRDA interfaces can be implemented via software programming. NEC coding, modulation, and demodulation are used by this interface. The frequency of modulated carrier signal is 38KHz, while the duty ratio of the square wave is 1/3. The length of data transmission, which is around 1m, is determined by two factors: one is the maximum value of rated current, the other is internal current-limiting resistance value in the infrared receiver. The larger the resistance value, the lower the current, so is the power, and vice versa. The transmission angle is between 15° and 30°, and is mainly determined by the radiation direction of the infrared receiver.

Notes:

Among the eight interfaces mentioned above, most of them can be multiplexed. Pin definitions that can be defined is not limited to the eight ones herein mentioned, customers can self customise the functions of the pins according to their specific application scenarios. Functions of these pins can be implemented via software programming and hardware.

2.5. Pin Definition for LED Light and Button

ESP8266EX features up to 16 GPIOs, all of which can be assigned to realise various functions of LED lights and buttons. Definitions of some GPIOs that are assigned with certain functions in our demo application design are shown below:

Pin Name	Function Name	Type	Pin Num
MTCK	Button (Reset)	I	12
GPIO0	WiFi Light	O	15
MTDI	Link Light	O	10

Table 15 Pin Definitions of LED and Button

Altogether three interfaces have been defined, one is for the button, and the other two is for LED light. Generally, **MTCK** is used to control the reset button, **GPIO0** is used as an signal to indicate the WiFi working state, **MTDI** is used as a signal light to indicate communication between the device and the server.

3. SCH and Layout

ESP8266EX is very highly integrated SoC which encapsulates Xtensa LX106 core processor, RAM, RF components and allow WiFi TCP/IP stack to be implemented on board with just few components beside ESP8266. The chipset also incorporates built-in self-calibration to compensate for performance errors, improving the modulation accuracy and stability of wireless communications.

High integration level of this chipset tremendously decreases the number of components used in peripheral circuit design. Beside ESP8266EX, only a number of less than 10 resistors and capacitors, one crystal oscillator, and one SPI Flash is needed to make a complete module with wireless communication capability. A detailed description of ESP8266EX schematics and layout design are illustrated here.

3.1. Circuit diagram (SCH)

The complete SCH of ESP8266EX is illustrated in Figure 3:

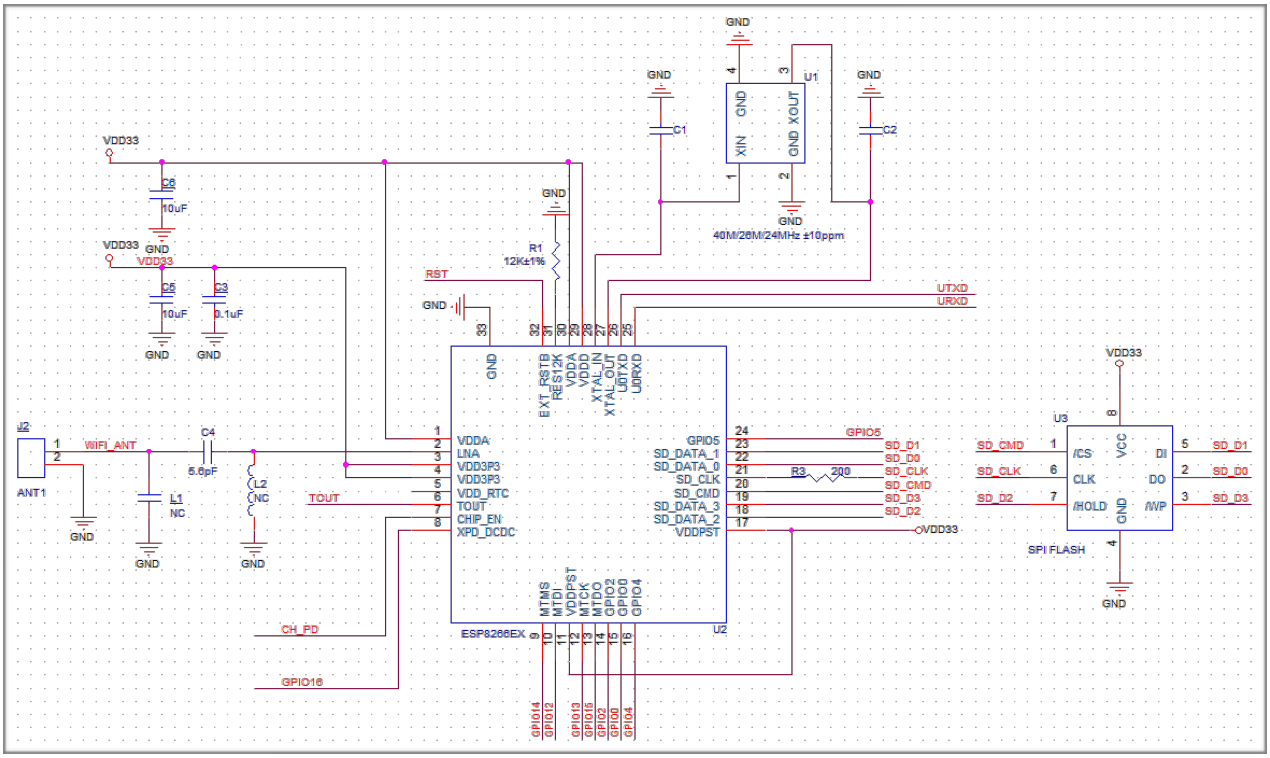


Figure 3 ESP8266EX SCH

ESP8266EX SCH design covers the following 5 parts:

- Power supply;
- power on sequence and reset;
- Flash;
- Crystal oscillator;
- RF.

1. Power-supply Pins

Digital Power-supply Pins

ESP8266EX has only two digital power-supply pins (abbreviated as VDDPST in the circuit diagram), Pin11 and Pin17. In digital power supply, there is no need to add additional filter capacitors. The operating voltage range of digital power-supply pins is between 1.8V and 3.3V.

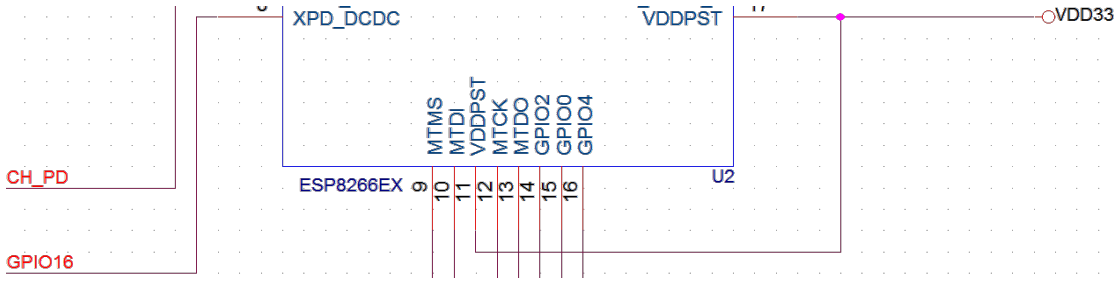


Figure 4 ESP8266EX Digital Power-supply Pins

Analog Power-supply Pins

ESP8266EX has 5 analog power-supply pins (abbreviated as VDD33 in the circuit diagram), including Pin 1, Pin 3, Pin 4, which provides internal power supply for internal PA and LNA respectively, and Pin 28, Pin 29, which supplies power for internal PLL. The operating voltage range of the analog power-supply pins is between 3.0V and 3.6V.

It should be noted that the power supply channel might be damaged due to the sudden increase of current when ESP8266EX is transmitting analog signals. Therefore, an additional 0.1uF capacitor with a package size of 0603 or 0805 is needed in circuit design. This capacitor can be used in 0.1uF in match with capacitor with 0.1uF capacitor with the package size of 0402.

(Notes: There is no need to add magnetic beads in the design of analog power-supply circuit, for ESP8266EX's EMC is in conformity with FCC and CE requirements, and has been approved.)

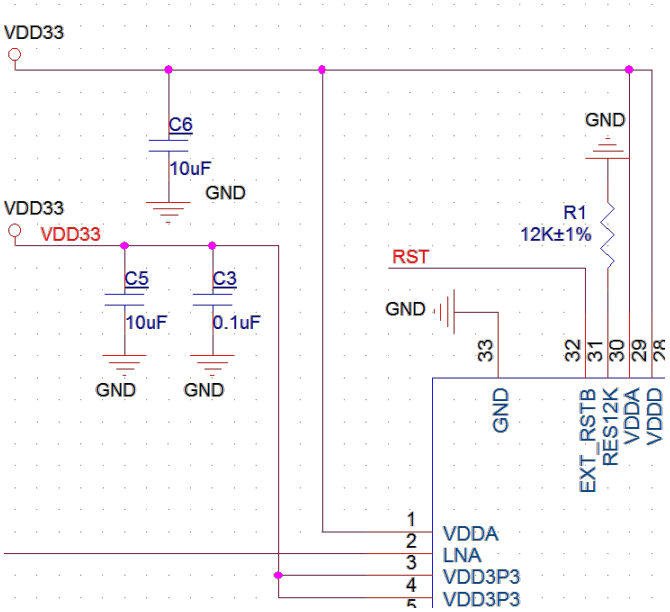


Figure 5 ESP8266EX AVDD

2. Power-on Sequence and Power Reset

Power-on sequence

The voltage of ESP8266EX's power supply systems is 3.3V, therefore only one rule should be abide by when you power on the device: Pin7 CH_EN, the power enable pin, should be powered on at the same time when or after the power supply system is powered on.

Note: If the power management IC is connected with the power-on enable pin CHIP_EN, it can control the power on-and-off of ESP8266EX by output high and low voltage through its GPIOs. However, pulsed current might be produced at the same time. In order to delay the transmission of pulsed signal and avoid unstable current of CHIP_EN, a RC time-delay circuit (R=1kΩ, C=100nF) is needed. There is an internal pull-up in the CHIP_EN pin, so no external pull-up is needed.

Reset

There exists internal pull-up resistor in the reset pin, Pin32, which can be left dangled when it is not used. When the chip is enabled, the reset pin is held low. In order to avoid reset caused by external interference, the lead is generally required to be short, and no external pull-up resistor is necessary.

The enable pin CH_EN (pin 7) can also serve as a reset pin. If voltage for CH_EN pin is low, the chipset ESP8266EX will power off. Note that this pin cannot be dangled.

3. Flash

Currently, the size of flash that we use in our demo is an SPI Flash, the ROM size of which is 512KB,and the package size is SOIC_8 (SOP_8).

A resistor (package size: 0402) is connected to Pin21, the SD_CLK pin via serial port, with the aim to lower the driving current, decrease the interference of serial communication and external interruption, adjust the sequence, and so on. The initial value of the serial connection resistor is 200 ohm.

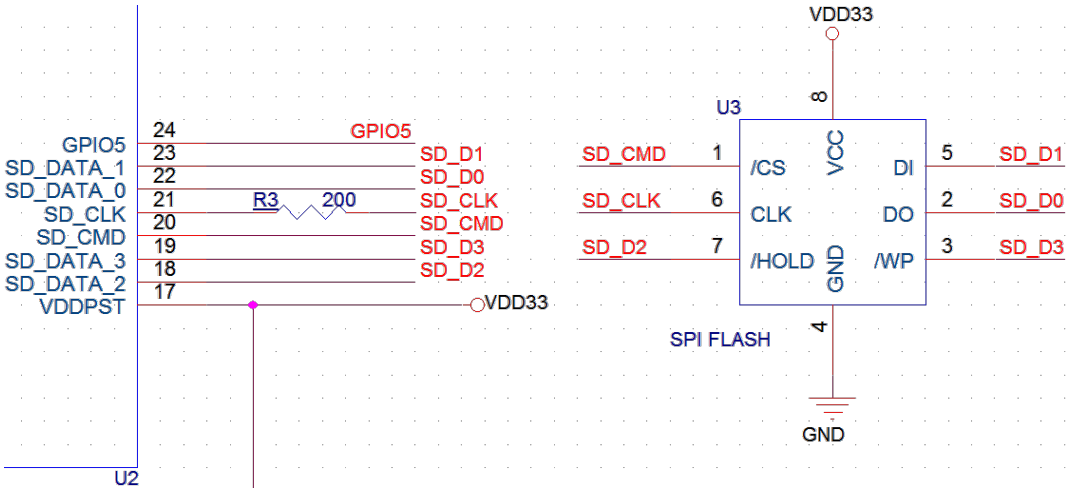


Figure 6 ESP8266EX Flash

4. Crystal oscillator

Currently, the frequency of crystal oscillators supported include 40MHz, 26MHz and 24MHz. The accuracy of crystal oscillators applied should be ±10PPM, and the operating temperature range should be between -20°C and 85°C.

When using the downloading tools, please remember to select the right crystal oscillator type. In circuit design, capacitors C1 and C2, which are connected to the earth, are added to the input and output terminals of the crystal oscillator respectively. The values of the two capacitors can be flexible, ranging from 6pF to 22pF, however, the specific capacitive values of C1 and C2 depend on further testing and adjustment on the overall performance of the whole circuit. Normally, the capacitive values of C1 and C2 are within 10pF if the crystal oscillator frequency is 26MHz, while the values of C1 and C2 are 10pF<C1, C2<22pF if the crystal oscillator frequency is 40MHz.

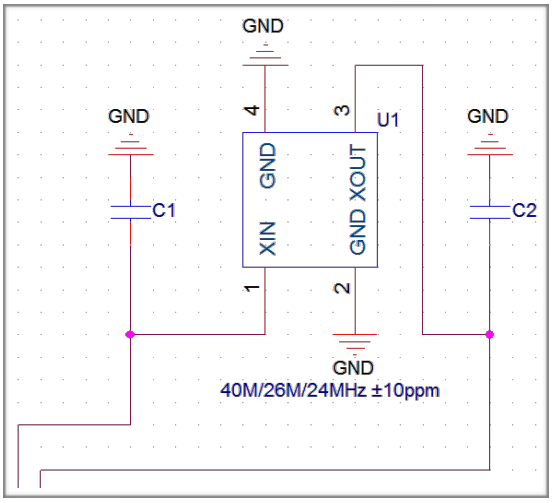


Figure 7 ESP8266EX Crystal oscillators

Note: Defects in the craftsmanship of the crystal oscillators (for example, high frequency deviation, unstable working temperature) may lead to the malfunction of ESP8266EX, resulting in the decrease of overall performance.

5. RF

The output impedance of RF pin (Pin 2) is 50 ohm. Normally, when the antenna impedance approaches 50 ohm, antenna matching is not necessary. However, low-price antenna commercially available in the market does not feature 50 ohm impedance. Besides, the impedance in 2.4G to 2.5G frequency band is rather scattered. Therefore, N-type matching network is essential in circuit design to facilitate antenna matching.

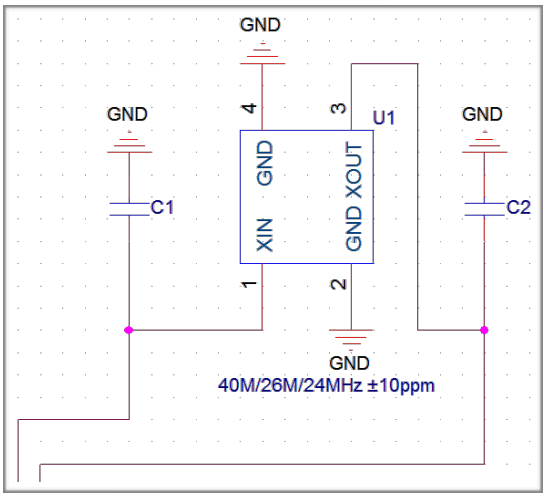


Figure 8 ESP8266EX RF

6. External Resistor 12K

An external resistor that is connected to the ground should be added to ERS12K pin (Pin31), so as to control the bias current in the circuit. Therefore, relatively high resistance value accuracy is required, an accuracy of 12K±1% is recommended.

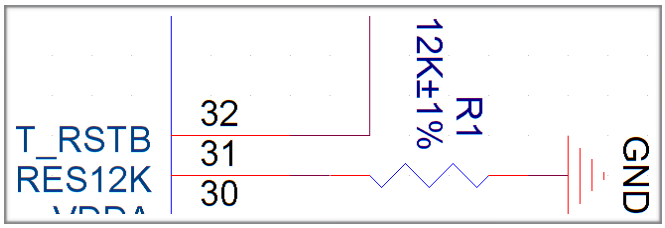


Figure 9 External Resistor

3.2. Layout design

PCB layout design of products using chipset ESP8266EX is demonstrated in this part. Hereto we mainly focus on two kinds of designs, one is ESP-WROOM serial to WiFi modules, and the other is main board mounted with ESP8266EX WiFi module.

1. ESP8266EX Module Design

- **Module layout design and the key techniques:**

This printed circuit board has four layers.

The first layer is the TOP layer, signal lines and components are placed on the top of the printed circuit board;

The second layer is the GND layer, no signal lines is laid so as to ensure an entire plain GND plane;

The third layer is the POWER layer, only power lines can be placed on this layer. However, there is exceptional cases. When there is no other choice but to place some signal lines on this layer, it is acceptable.

The forth layer is the BOTTOM layer, only signal lines are designed on this layer, no components shall be placed on this layer.

- **On design of the power-supply part**

The power supply voltage of those signal lines highlighted in yellow is 3.3V. The total width of the power line shall be larger than 15 mil.

Before the power line reaches the analog power-supply pins (including Pin 1, 3, 4, 28, 29) of ESP8266EX, a 10uF capacitor with 0603 or 0805 package needs to be added, as is illustrated in Fig. 10. C6, which is the capacitor, should be placed adjacent to the analog power-supply pins of the chipset.

Power lines should be placed on the third layer. When the power lines reached the pins of the chipset, VIAs are needed so that the power lines can go through the layers to connect the pins of the chipset on the TOP layer. The diameter of the VIA holes should exceed the width of power lines, while the drill should be appropriate, a little bit larger than the radius of VIA is enough.

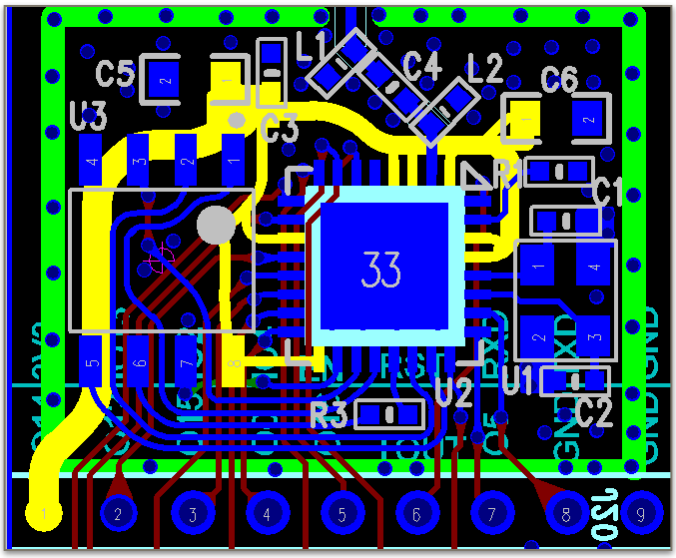


Figure 10 ESP8266EX PCB Layout

- **On design of the crystal oscillator**

Crystal oscillator should be placed adjacent to the XTAL Pins, the connection lines shouldn't be too long, and should be wrapped up for shelter.

The input and output lines cannot be punched, cannot cross the layers or be crossed.

The input and output bypass capacitor should be located near the chip; never set it on the lines.

No high frequency digital signal lines shall be placed under the four layers of the crystal oscillators. The best choice is that no signal lines is placed under the crystal oscillator. The TOP layer where is crystal oscillator is placed should be as large as possible.

Magnetic components, such as high current inductors, should not be placed near to crystal oscillator, a sensitive component.

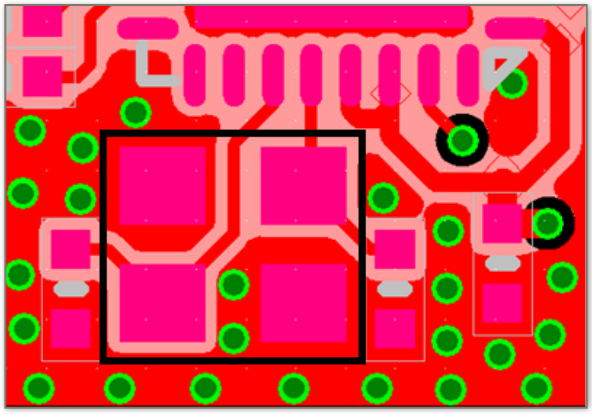


Figure 11 ESP8266EX crystal oscillators PCB layout

- **On design of the RF part**

The characteristic impedance that RF lines should control is 50Ω, in order to ensure the complete board in the second layer. The surrounding drilled hole should be blocked and the lines should be as short as possible.

A π matching circuit near the RF Pin should be reserved in RF lines. RF lines connecting the chip and antenna should not cover drills, which means cross layer lines are not allowed.

The width of RF lines should not be less than 6 mil and should keep up to10 mil.

RF lines should not be set at a vertical, or a 45-degree angle. Circular lines are allowed if necessary.

No signal lines of high frequency should be set near RF lines.

RF antenna should be set away from high frequency transmitting devices, such as crystal oscillators, DDR, and certain high frequency clocks (SDIO_CLK, etc).

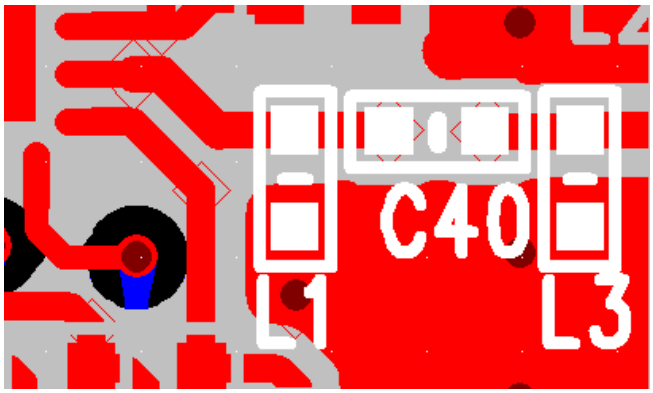


Figure 12 ESP8266EX RF PCB layout

2. ESP8266EX slave design

When ESP8266EX is matched with CPU as a slave unit, information integrity in layout design is more important than that in analogue design.

Due to the system accountability, the increasing high frequency signals would result in interference in ESP8266EX. Attentions should be paid to those interferences.

Main boards in PAD or TV BOX will be discussed.

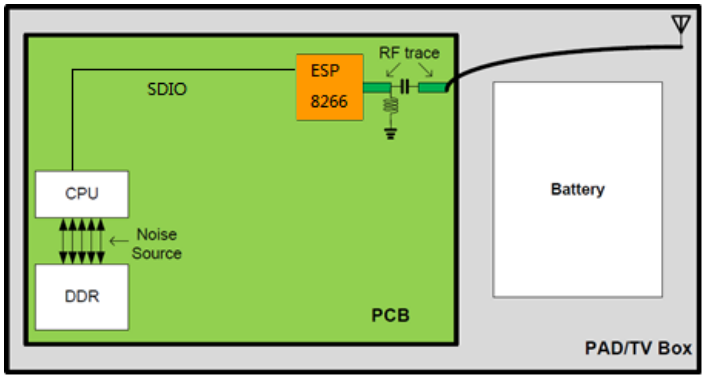


Figure 13 Planning framework of layout plane position

The digital signals between CPU and DDR produces high frequency noise and will interference WiFi frequency in the air. Therefore, the following points should be noted in system designs:

- As shown in Fig.4, ESP8266EX is on the edge of PCB and far away from CPU and DDR(the noise source CPU+DDR). The increase in distance will decrease the interference distance and would reduce the coupling noise;
- When ESP8266EX communicates with CPU via SDIO, it would be optimal if the six signal lines are connected through a 200Ω series resistor. The purpose is to reduce the drive current and the corresponding interference and at sthe same time sequence problems due to the inconsistent length of SDIO lines.
- PCB onboard antenna should not be selected as it receive relatively large interferences and is vulnerable to the coupling noise that might affect RF performance. External antenna should be applied that can be directed away from the PCB board so that the influence of interference signals of high frequency on WiFi will be reduced.
- During layout, the high frequency signal line control between CPU and MEM should be noted. The line layout should comply firmly with high frequency signal regulations (refer to DDR line control documents) where CLK should be lined underground, data lines and addr lines should be packed and lined underground.
- The GND of WiFi circuit and other high power devices should be separated and connected through wires if there are electric machines in system design.
- Antenna should keep away from noise source of high frequency, such as LCD, HDMI, Camera Sensor, USB and other high frequency signals.

3. FAQ in design

1. Typical phenomenon: The current ripple is not large, but the TX performance of RF is rather bad.

Problem description: ripple has a strong impact on the performance of RF TX. It should be noted that ripple must be tested when ESP8266EX sends normal packets. The ripple increases when the power gets high. Generally, the ripple value should <120mV when sending the packet 11N MCS7the ripple value should <200mV when sending the packet 11B 11M.

Solution: add a10uF filter capacitor to the branch of source circuit (ESP8266EX AVDD pin). 10uF capacitor should be placed adjacent to the AVDD pin. The ripple is much small and more stable when it's near the pin.

2. Typical phenomenon: when the chipset is sending data packages, the power ripple is small and the TX performance of the RF is not good

Problem description: the poor TX performance of the RF is not only caused by the problematic power ripple, but also by abnormal crystal, for example, the crystal itself is of low quality and the crystal frequency offset is too big (when over ±40PPM, the ESP8266EX will not be able to work properly and the performance will get worse accordingly); or the crystal has been interfered with high frequency signals, for example, the input signals couple with the output signals or the output signals couple with the input signals due to the cross wiring of input and output signal wires at different layers; or high frequency signal wires are wired below the crystal such as the SDIO wiring and UART wiring, which will cause malfunction of the crystal. Another problem that has not received due attention is the existence of inductive or radioactive parts beside the crystal, for example, great inductance, antenna (many designers, when considering the area of the ESP8266EX module, often place the crystal very close to the PCB on-board antenna, which, at the time ESP8266EX module sends data packages, will lead to direct coupling between radioactive interference and the crystal, the crystal and the antenna, thus resulting in very poor performance of the RF).

Solution: this problem is mainly caused by inconsiderate layout and can only be solved by re-layout. See Chapter 2.7.2 for details about layout.

3. Typical phenomenon: when ESP8266EX is sending data packages, the power value tested by an instrument is much higher or lower than the target power value, and the EVM is relatively poor

Problem description: the sharp difference between the power value tested by an instrument and the target power value is largely caused by the mismatch of the resistance in the section from the chipset RF pin to the antenna. That is to say the resistance in the section from the chipset RF pin to the antenna deviates from the 50Ω a lot, leading to reflections during signal transmission. The reflections can be divided into positive reflection and negative reflection. When the resistance in the section from the chipset RF pin to the antenna is larger than 50Ω, positive reflection will be formed and the power will grow bigger than normal; if the resistance is smaller than 50Ω, negative reflection will be

formed and the power will become smaller than normal. By the way, mismatch of the resistance will affect the performance of the PA within the chipset, leading to PA's premature entry into the saturation regions, thus resulting in large distortion of the signals and according poor EVM performance.

Solution: leave a π shaped circuit on the RF wiring, which shall allow match of the resistance with the antenna, so as to enable the resistance in the section from the chipset RF pin to the antenna to approximate 50Ω.

4. Typical phenomenon: TX performance is not bad, but the RX sensitivity is rather high.

Problem description: Good TX performance means proper RF impedance matching. RX performance is strongly influenced by the external interference coupling to the antenna. As modules pose no other high frequency signal coupling to the antenna, RX sensitivity is thus not influenced except when crystal oscillators are set near the antenna, or UART TX and RX conducts through RF trace lines. If ESP8266EX serves as slave, there will be quite a number of high frequency interference. Therefore, signal interference depends on board design.

Solution: keep the antenna away from crystal oscillators and keep RF trace lines away from high frequency signal.

3.3. Development Board

Espressif Systems provides ESP8266EX development board for quick evaluation and familiarisation of products and for secondary development for customers. Refer to Fig.7 for layout (size: 46x78.5mm) and interface specification.

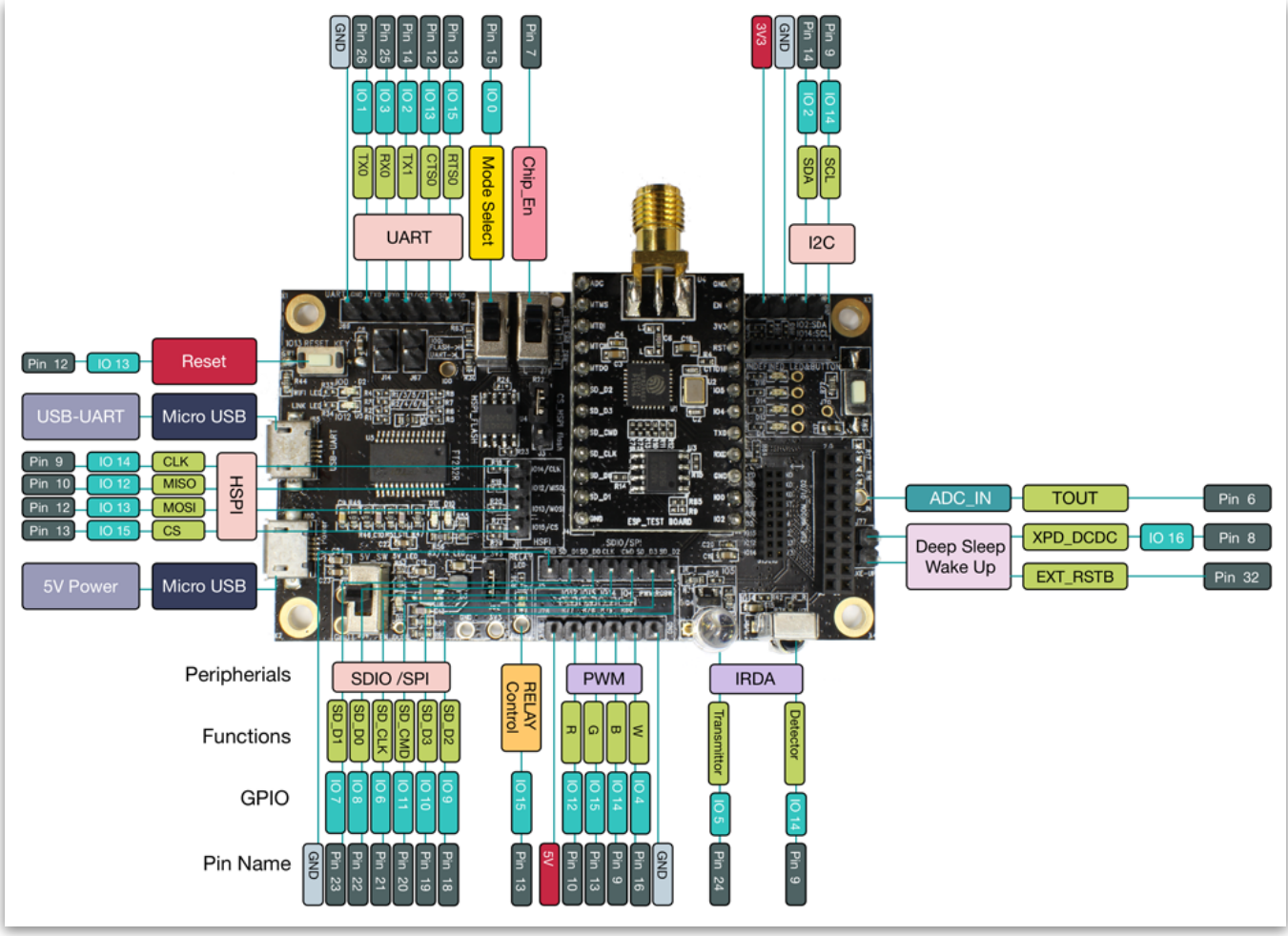


Figure 14 ESP8266EX development board diagram

Type	Specification
USB Interface	Mini USB or Micro USB can be applied to serve as 5V power supply or as communication.
5V Power-supply	USB power supply that can be connected to rear circuit by 5V power switch.
3.3V Power-supply	DC/DC regulator transfers 5V into 3.3V for partial WiFi circuit. There is a power indicator at 3.3V power supply and a plunger pin for test power current.

Item	Name	Functional specification
J 11	H SPI	Can be used to connect external SPI Flash (Flash2), display, and MCU, etc.
IO15	Relay Control	The terminal that a smart plug can control the power on and off of a relay. An indication light is equipped.
J5	SDIO/SPI	Can be connected to the Flash, MCU HOST and display ,etc.
J78	PWM	Provides 4 PWM output and can control smart lights.
D15, U7	IRDA	Application for infrared emission (D15) and reception (U7).
ADC_IN	ADC_IN	Can be used to test analogue input voltage and sensors.
J68, J83, J84	I2C	Can be applied to external sensors and display with 2.54 and 1.27 ports.
J69	UART	UART0: U0TXD, U0RXD, MTDO(U0RTS), MTCK(U0CTS) UART1: GPIO2(U1TXD)
		Downloading: U0TXD+U0RXD or GPIO2+U0RXD Communication: U0TXD, U0RXD, MTDO(U0RTS), MTCK(U0CTS)
		When using U0RTS and U0CTS, jumper cap is needed for short circuit for J14 and J67. If the print output affects the corresponding function when U0TXD is powered on, U0TXD, U0RXD and MTDO(U0RTS), MTCK(U0CTS) can be interchanged. Indirect shield and print. Debug: GPIO2(U1TXD) can be printed as debug information.
J64	Button or switch	5V power switch
J79		CH_PD switch
J66		GPIO0 transfer to downloading mode switch
SW1		A reset button that connects to MTCK(GPIO13) for the reset of IOT application.
SW2		The reset button can be defined by the user.
D2	Indicator light	Red light (D2) is an indicator light for the working condition of WiFi.
D3		Blue light (D3) is an indicator light for the communication of the server.
D11		Active indicator light for RX and TX respectively.
D12		Indicator light 3.3V power supply.
D4/13/14/16		Can be defined by the user.

Table 16 Descriptions on the Pins of the Development Board

Miscellaneous:

- When the device is working under the power-saving mode, i.e., deep sleep mode, GPIO16 should be connected to EXT_RSTB (here refers to J77) so that the device can be waked up. Besides, the EXT_RSTB can also be connected to the GPIOs of an external MCU so as to wake up the device.
- When using the buttons or switches, pull-up means the device is powered on, while pull-down means that the device is connected to the ground. When downloading, the button that controls GPIO0 should be pulled down, while the button that controls Flash boot should be pulled up.
- There are two SPI Flashes on the development board, Flash 1 and Flash 2. They are used store firmwares of the application programs.

  Flash1: connected through the SPI interface. When the device is working under the standabloe mode, Flash1 is mainly used. The CS of Flash 1 can be decided by R9 and R85 on the development board. By default Flash1 is enabled.

  Flash2: connected through the H SPI (multiplexing GPIO) interface. In the design of the demo development board, SDIO/ SPI serves as slave and connects to an external MCU. H SPI is used to connect Flash2. Flash 2 can be chosen by J3.

Instructions for the development board:

Name	Instructions
SMA	generally used to connect external antenna and can also be used to connect development board to test instruments for RF performance test via cable wires.
SDIO	connects to external devices
COM12x2_2.54	compatible to breadboard for separate development and debugging.
1.27 Module interfacce	can be connected to external DIP modules with 1.27mm needle spacing.
2.0 Module interfacce	compatible to DIP module ESP-WROOM-01 with 2.0 mm needle spacing and SMD module ESP-WROOM-02 (with pinboard)
Test point	5V, 3V3, GND, IO15, IO0, CH_PD, ADC_IN. External test hook can be added for test connection.
Locating hole	X1, X2, X3, X4

Table 17 Instructions on the Development Board

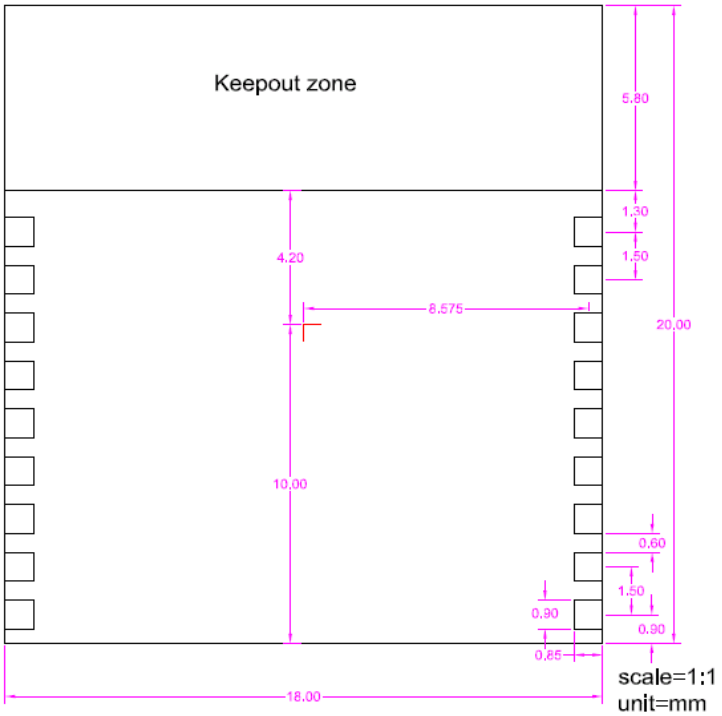
Notes: Firstly, please pay close attention to the indicators of the Pin-outs for each of them shall be connected correspondently. Secondly, the two types of modules introduced hereafter should not be used simultaneously.

3.4. ESP-WROOM Serial WiFi Modules

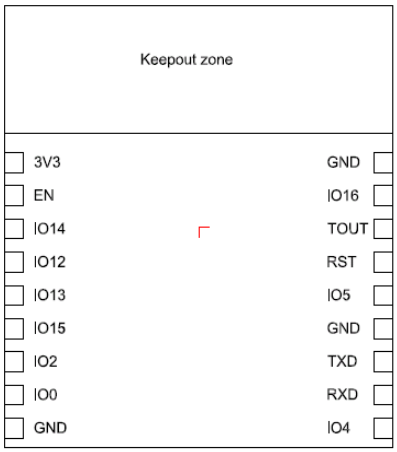
Espressif Systems offers 2 types of modules: SMD and DIP. Both of them have been tested to achieve optimal RF performance. ESP-WROOM Serial WiFi Modules provided by Espressif Systems are highly recommended for beginners who want to do initial performance test and secondary development.

1. SMD Module - ESP-WROOM-02

The pin definitions and distribution of the SMD Module is illustrated in Figure 16. The external size of the module is 18*20mm. The type of flash used on this module is an SPI flash, the package size of which is SOP8-150mil, the antenna applied on this module is a 3DBi PCB-on-board antenna.



Module Dimension
(Top view)



Module pinmap
(Top view)

Figure16 SMD Module - ESP-WROOM-02

There are altogether 18 pin-outs, the distribution and definitions of which are listed below:

NO.	Pin Name	Function
1	VDD	3.3V Power Supply
2	EN	Chip Enable. Active high.
3	GND	Ground
4	RST	Module reset
5	TOUT	ADC pin
6	RXD	UART0_RXD; GPIO3
7	TXD	UART0_TXD; GPIO1
8	IO0	GPIO0
9	IO2	GPIO2; UART1_TXD
10	IO4	GPIO4
11	IO5	GPIO5
12	IO12	GPIO12; HSPI_MISO
13	IO13	GPIO13; HSPI_MOSI; UART0_CTS
14	IO14	GPIO14; HSPI_CLK
15	IO15	GPIO15; MTDO; HSPICS; UART0_RTS
16	IO16	GPIO16; Deep-Sleep Wakeup

Table 18 Pin Definitions of ESP-WROOM-02 WiFi Module

Connect the 3.3V power-supply pin to an external 3.3V power source, for 3.3V is the power-supply for both analog circuit and digital circuit.

When working, normally the voltage level of the EN pin, WiFi enable pin, should be set high.

SMD Module features two working modes: one is UART Download mode, the other is Flash Boot mode. UART Download mode means that user programs can be written into the Flash or Memory by flash downloading tools. If the programs are burnt into the Memory, the programs can run only when the device is powered on, once the device is powered off, the programs in the Memory will be erased. However, when the programs are burnt into the Flash, they will be stored in it, and can be invoked and used at any time.

Before the module is powered on, pin GND RXD TXD should be lead out, and be connected with USB to TTL serial cable so as to download, print log and communicate.

By default the Flash is empty. Therefore, the following procedures should be followed when you burn the programs into the Flash:

- Before burning, set the module to work under UART Download mode;
- Pull IO15 and IO0 to low-voltage level, leave IO2 dangled;
- Burning the programs into Flash;
- Burning the program into Flash using flash downloading tools;
- After burning the programs into Flash, pull down IO15 to low-voltage level, keep IO2 dangled, and pull up IO0 to high-voltage level. The module is then shifted from UART Download mode to the Flash Boot mode;
- The initialisation would read and run programs from Flash after it is powered on.

Note:

- The whole operating process can be examined through the log information printed by UART interface. If the programs written into the Flash do not function in the right way, please check the initial settings of the working mode through logs printed from a serial port.
- Serial printing tools (for example, SecureCRT) and flash downloading tools cannot open the serial port simultaneously.

2. DIP Module - ESP-WROOM-01

The DPI type module - ESP-WROOM-01 is illustrated in the picture below.

The size of the module is 18*19mm, the Flash type applied is a SPI flash packed in SOP8-150mil, the antenna used is a 1 DBi metal antenna. The 2.00mm double pitch applied can be both vertical or straight, depending on specific applications.

Please refer to Table 18 for pin definitions of this module.

Note: The DIP metal antenna is thin and prone to distortion. Change the antenna immediately if the shape and appearance are abnormal.

4. Typical Application Examples

4.1. WiFi smart hardware converted from UART serial ports

The pins on basis of the 2 UART ports are defined below:

Category	Pin Definition	Function
UART0	(Pin 25) U0RXD+ (Pin 26) U0TXD	Can be used to receive and send the users' data packages
UART1	(Pin 14) GPIO2 (U1TXD)	Can be used to print information

Table 19 Pin Definitions of 2 UART Interfaces

AT+ instructions and instruction sets documentations are provided for the relevant software.

Application example: ESP8266EX development board as shown in Figure14.

4.2. Sensor

ESP8266EX can be used to develop sensor products and the interface used is I2C interface. Under this condition, I2C is working with Master mode and is connected to multiple sensors, communicating through addressing mode which identifies Slave device (every slave device has a unique address identity).

Such sensor products will send real-time data through I2C interface to ESP8266EX which will upload the data to the server wirelessly. When an mobile phone is connected to the public internet, it can access the data on the server through an app.

4.3. Smart light

ESP8266EX can be used to develop smart home products such as smart LED lights which use PWM interfaces and infrared interfaces. The 3 PWM interfaces control the red, blue, green LED lights respectively. Theoretically speaking, the minimal PWM duty ratio can reach 1/256, thus supporting 256*256*256 types of colors. Besides, the infrared interfaces allow specific control over LED lights, for example, reset, on/off, adjustment of the color.

4.4. Smart plug

ESP8266EX can be used to develop smart home products such as smart plugs which use ordinary GPIO interfaces. GPIO interfaces allow control over high and low levels as well as connection and disconnection of relay, thus allowing smart control over plug on/off. This application is mainly comprised of 3 modules which are: 220V to 5V power module, ESP8266EX WiFi module and relay control module.

Other Technical Documents

Please contact Espressif Systems if you need more information about ESP8266EX IoT solution.

Hardware:

We have data sheets, reference design, schematics and PCB layout, BOM list and so on.

Software:

- Espressif IoT SDK User Guide, which introduces to you how to establish the development environment.
- Espressif IoT Demo User Guide, which introduces to you how to debug and test demos provided.
- Espressif IoT SDK Programming Guide, which introduces to you all the software interfaces.
- Espressif Cloud Introduction, which introduces to you how to apply our Cloud service.
- Espressif Flash RW Operation Guide, which teaches you how to read and write the Flash.
- Espressif Timer, which explains on how to implement the timing function of the Cloud server.
- Mass Production Testing Solution, which offers you guidance on how to execute automatic test before mass production.